A High-Power Broadband Passive Terahertz Frequency Doubler in CMOS

Ruonan Han, *Student Member, IEEE*, and Ehsan Afshari, *Senior Member, IEEE*

***Abstract*—To realize a high-efficiency terahertz signal source, a varactor-based frequency-doubler topology is proposed. The structure is based on a compact partially coupled ring that simultaneously achieves isolation, matching, and harmonic filtering for both input and output signals at f_0 and $2f_0$. The optimum varactor pumping/loading conditions for the highest conversion efficiency are also presented analytically along with intuitive circuit representations. Using the proposed circuit, a passive 480-GHz frequency doubler with a measured minimum conversion loss of 14.3 dB and an unsaturated output power of 0.23 mW is reported. Within 20-GHz range, the fluctuation of the measured output power is less than 1.5 dB, and the simulated 3-dB output bandwidth is 70 GHz (14.6%). The doubler is fabricated using 65-nm low-power bulk CMOS technology and consumes near zero dc power.**

***Index Terms*—CMOS, conversion efficiency, frequency doubler, passive, ring structure, signal source, terahertz, varactor.**

I. Introduction

TERAHERTZ frequency range (300 GHz$\sim$3 THz) is very attractive for numerous applications in security, biomedical imaging, spectroscopy, and high-speed data transmission [1]–[7]. In particular, signal generation at milliwatt level using CMOS circuits is critical for affordable, lightweight, and highly integrated terahertz systems. Unfortunately, we are limited by the cutoff frequency, $f_{\max}$, of the transistors, which is only about 200 GHz (with device interconnects) even in advanced CMOS technology nodes [8]. This poses a theoretical constraint beyond which fundamental oscillation and power amplification cannot be performed [9]. Meanwhile, because of the lossy silicon substrate, low metal thickness, and close proximity between top and bottom metal layers, it is hard to build high quality-factor passive structures and high-impedance transmission lines [10]. Finally, with the ever-decreasing breakdown voltage of the devices in deep-submicron CMOS technologies, voltage swing (thus, output power) of terahertz circuits is severely limited. All these issues make the high-power generation in the terahertz range from CMOS circuits very challenging. Thus, high-power signal sources are traditionally fabricated using compound semiconductor processes (e.g., GaAs and InP) [11]–[15].

Consequently, utilizing harmonics is probably the only solution to generate signals at terahertz range in CMOS. Generally, there are two approaches to achieve this task, which are: 1) harmonic extraction from an oscillator and 2) low-frequency source cascaded with a frequency multiplier chain. While it is a subject of debate which method generates higher power, the former is normally more compact and power efficient as fundamental oscillation and harmonic generation occur simultaneously. In [16], the output power of -7.9 dBm at 482 GHz is reported in an oscillator utilizing the optimum oscillation condition of the two-port network. In [17], -7.2 dBm at 280 GHz is demonstrated in a 16-element distributed active radiator (DAR) array. In [18] and [19], power of -1.2 dBm at 290 GHz is generated from four unidirectionally coupled oscillators. On the other hand, as the fundamental oscillation frequency approaches $f_{\max}$, the parasitic capacitance of the switching transistors becomes a dominant portion in the resonance tank, giving very little room for the frequency tuning, which is required in applications like spectroscopy [20]. The largest achieved tuning range in terahertz harmonic oscillators is only 4.5% [18], [19]. Alternatively, we can use a lower frequency source to feed a multiplier chain to achieve broader tuning range. However, all the previously reported CMOS frequency multipliers near or at terahertz range are based on active components (e.g., transistors) so they consume a considerable amount of dc power [8]. Moreover, the highest output frequency of the state-of-the-art CMOS multipliers is only 275 GHz [21], [22], and the conversion loss could rapidly increase if the operation frequency goes up.

To build high-power terahertz sources, the goal of this work is to exploit the method of multiplier chain with the focus of the design of a terahertz frequency doubler [24]. To eliminate the problem of high power consumption in the existing CMOS multipliers, the proposed doubler is purely passive and exploits MOS varactors to generate nonlinearity. Meanwhile, the doubler is optimized in terms of conversion efficiency, output power, and bandwidth. To achieve this, in Section II, a novel and effective ring structure for a terahertz doubler is proposed. In Section III, a method to find the optimum matching conditions of MOS varactors for the highest conversion efficiency is presented. Based on these techniques, a 480-GHz frequency doubler is discussed and simulated in Section IV. After the experimental results in Section V, we summarize this paper in Section VI with a performance comparison with the state-of-the-art.

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The authors are with the Department of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14850 USA (e-mail: rh383@cornell.edu; ehsan@ece.cornell.edu).

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II. Terahertz Frequency Doubler: Ring Structure

There are at least three major requirements to achieve the highest conversion efficiency in a varactor-based frequency doubler.

1) The maximum amount of power at the input frequency f_0 needs to be injected into the varactors from the input source. At the same time, all the generated power at $2f_0$ should be extracted out of the varactors and delivered to the load. This requires the rest of the doubler structures to achieve simultaneous power matching from input to the varactors at f_0 and from the varactors to output at $2f_0$.
2) The doubler structure should prevent power leakage from input signals (f_0) to the output and from the generated signal $(2f_0)$ to the input; thus, effective isolation is needed at both sides of the doubler.
3) Since the metal structures in CMOS are lossy at the terahertz range, the doubler should remain as compact as possible. Normally, with fewer resonators, a compact structure also enhances the operation bandwidth.

Unfortunately, implementation of all these requirements in a single design is challenging. For example, a compact structure has very few parameters that can be tweaked; meanwhile signals at both f_0 and $2f_0$ would inevitably coexist in most parts of the structure so that optimizing one merit at one frequency would normally lead significant deviation of other merits from their optima. Namely, the degree of freedom in design is severely constrained.

To solve this problem, we propose a doubler topology based on a ring structure, as shown in Fig. 1(a). This ring is axial symmetric, and is based on grounded coplanar-waveguide transmission lines (GCPW TLs) [10]. Part of the left half of the ring, TL_0, is magnetically coupled to the input. The output is located at the central node of the right half of the ring. A pair of MOS varactors, C_{var1} and C_{var2}, are connected to the ends of two transmission-line branches, TL_2. Next, to understand the operation principle of this ring structure, the signal flows at f_0 and $2f_0$ are described in detail.

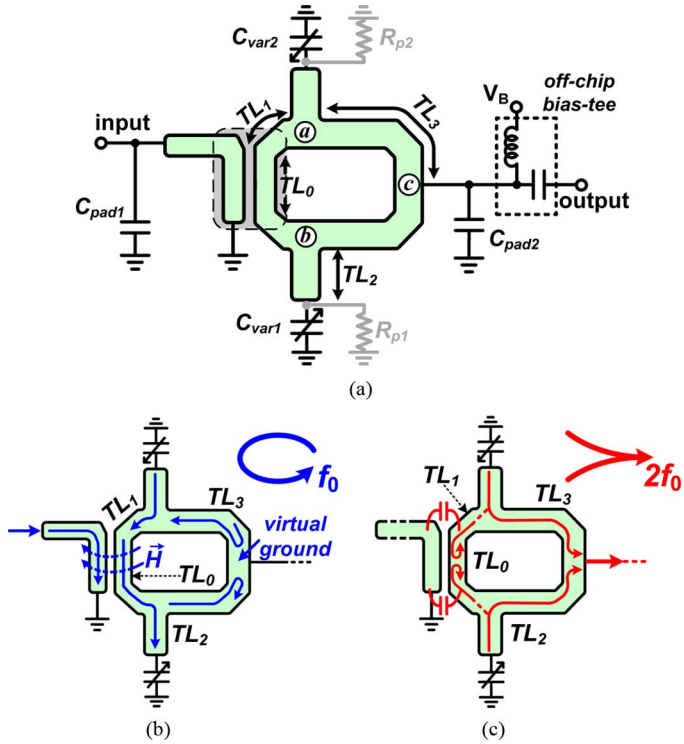


Fig. 1. (a) Proposed partially coupled ring structure for varactor-based terahertz frequency doublers. (b) Signal flow at fundamental frequency. (c) Signal flow at second harmonic.

A. Signal Flow at Input Fundamental-Frequency f_0

The signal flow at f_0 is illustrated in Fig. 1(b). The input signal creates a magnetic field circling around the coupled lines, TL_0, and induces differential currents rotating inside the ring. As the induced signals travel through the two branches, TL_2, they are then absorbed by the varactors and up-converted to $2f_0$. Some portion of the signals would continue traveling along the ring until it reaches the output node. Since the signals from the top and bottom of the ring are out of phase at this point, the output node behaves as a virtual ground at f_0, and reflects these signals back, resulting in standing waves in TL_3. The combination of TL_1, TL_2, and TL_3 achieves conjugate matching to the varactors, as will be discussed in detail in Section IV. This way, most of the input power can be differentially injected into the varactors from the input port with very little leakage to the output port.

B. Signal Flow at Output Second-Order Harmonic $2f_0$

For the signals at $2f_0$, the varactor pair functions as a power source [shown in Fig. 1(c)]. After the first-order self-mixing of the injected differential signals at f_0, both the frequency and phase of the signals are doubled by the nonlinear capacitors. Therefore, the signals at $2f_0$ coming out of the two branches are in phase, and after traveling along TL_3, they are combined constructively at the output node on the right. Part of the signal also flows into the coupled lines through TL_1, but the magnetic fields they created are out-of-phase so that no current is induced at the input feed line. The only leakage mechanism for signals at $2f_0$ is through the inter-line parasitic capacitance of TL_0, which is designed to be small (to be shown in Section IV). This way, the left half of the ring presents large impedance to the signals at $2f_0$ so that the output pad extracts most of the generated power at $2f_0$.

It can be seen from the above explanation that by guiding the signals at f_0 and $2f_0$ in different modes, paths, and directions, more design flexibilities are introduced. For example, the signal at f_0 is more sensitive to the left half of the ring, while the signal at $2f_0$ is more sensitive to the right half. Therefore, we can optimize the two halves of the ring independently for matchings at two frequencies. It can also be seen that the proposed ring structure, although compact, effectively enables the isolation of signals at f_0 and $2f_0$. Such isolation is normally difficult for varactor-based doublers because the varactor is a one-port device. Conventionally, in GaAs doublers, the isolation for the diode varactors is achieved using the electromagnetic (EM) mode orthogonality between the input TE_{10} balanced wave and the output TEM unbalanced wave [25]. This method, however, is not practical for CMOS doubler design because hollow-conductor waveguides can not be fabricated on chip, and the TE_{10} mode is not supported by the transmission

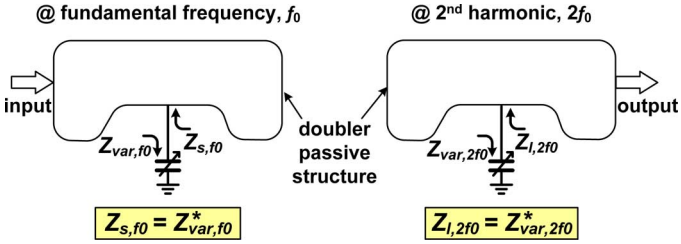


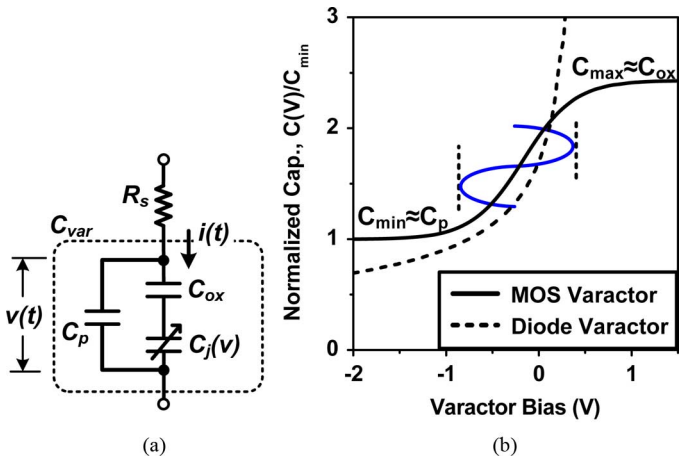
Fig. 2. Optimum matching scenarios of a general varactor-based doubler.

lines in CMOS. In contrast to varactors, isolation for a transistor-based doubler is easier because the transistor is a two-port device, of which the small inverse gain (S_{12}) can naturally isolate the generated second-harmonic signals from the input. Also, to prevent signal leakage, quarter/half-wave reflectors at input and output are commonly used [8], [23], [26], [27], which inevitably increases loss and reduces bandwidth. The proposed ring structure, however, eliminates the need for such reflectors.

The dc bias voltage of the varactors are applied externally through the output pad of the doubler ring, as is shown in Fig. 1(a). Resistors R_{p1} and R_{p2} are in shunt with the varactors to prevent gate–oxide breakdown by the accumulated charge during metal deposition. Their resistance is designed to be large so that both the RF loss introduced to the doubler and the dc power are negligible.

III. Optimum Matching Conditions

In any varactor-based doubler, what the passive metal structure ultimately presents to the varactor can be summarized into simply two parameters: the fundamental source impedance, Z_{s,f_0}, and the second-harmonic load impedance, $Z_{l,2f_0}$ (shown in Fig. 2). These impedances fully determine how efficient the varactor can convert the injected power at f_0 into the output power at $2f_0$; therefore, it is very important to find the optimum values for Z_{s,f_0} and $Z_{l,2f_0}$. For the most efficient power injection and extraction, the values of Z_{s,f_0} and $Z_{l,2f_0}$ should be the complex conjugates of Z_{var,f_0} and $Z_{\mathrm{var},2f_0}$, the varactor impedance at f_0 and $2f_0$, respectively. It is noteworthy, however, that due to nonlinearity and large-signal stimulus, Z_{var,f_0} and $Z_{\mathrm{var},2f_0}$ can be quite different from the small-signal $R_s - C_0$ impedances of the varactor, where R_s and C_0 are the series resistance and average capacitance of the varactor. For example, to inject power at f_0 into the varactor for frequency conversion, if we use small-signal matching, we incorrectly deliver maximum power into R_s, which represents varactor loss rather than any nonlinear doubling process. Thus, in this section, we will analyze the implication of the nonlinear frequency-doubling process from a circuit-design point of view. The mechanism of the varactor "absorbing" power at f_0 and "transferring" this power into $2f_0$ will be presented to explain how the matching at f_0 and $2f_0$ should be done. We will also show that the values of Z_{var,f_0} and $Z_{\mathrm{var},2f_0}$ are interdependent. Due to such interdependency, parametric sweeps using a simulator for searching the optimum matching conditions are complex (if not "blind") and time consuming. This makes it more desirable to find an analytical method to directly obtain the optimum Z_{s,f_0} and $Z_{l,2f_0}$ as at least a good starting point.



(a) (b)

Fig. 3. (a) Equivalent circuit of a MOS varactor. (b) Simulated C–V curve of an accumulation-mode MOS varactor in a 65-nm CMOS process. In comparison, the linear region of the C–V curve of an ideal abrupt-junction diode ($\phi_i = 0.3$ V) is much smaller.

The classic theories developed in the 1950s and 1960s [28]–[31] are based on devices with abrupt or graded semiconductor junctions of which the nonlinear capacitance is described by [32]

$$C_j(v) = \frac{C_{j0}}{\left(1 - \frac{v}{\phi_i}\right)^{\gamma}} \tag{1}$$

where C_{j0} is the zero-biased capacitance, ϕ_i is the junction built-in potential, and γ is the junction grading coefficient ($\gamma = 0.5$ for abrupt junction). Based on (1), the prior works [28]–[31] predict the efficiency with high precision. However, the results are too complicated to be useful in circuit design. Moreover, these works do not provide an intuitive methodology to design an optimum frequency multiplier that achieves the highest conversion efficiency. For the accumulation-mode MOS varactors used in this paper, the capacitance-tuning mechanism is based on the depletion-layer modulation described in (1); however, in addition to $C_j(v)$, the overall capacitance also includes two constant portions: the series gate–oxide capacitance, C_{ox}, and the shunt interconnect parasitics, C_p [see Fig. 3(a)]. The capacitor C_{ox} degrades the slope of the C–V curve of C_j at the higher bias voltages, and therefore greatly extends the linear range of the overall C–V curve [see Fig. 3(b)]. Meanwhile, C_{ox} and C_p also set harsh upper and lower bounds, which confine the capacitance nonlinearity in between. Therefore, compared to the varactors solely based on junctions (e.g., Schottky diode), the effective nonlinearity of MOS varactors can be better approximated to the first order within the bounded region

$$C_{\mathrm{var}}(v) = C_0(1 + bv) \tag{2}$$

where C_0 is the average capacitance, and b is the slope of the C–V curve. Next, we use the fundamental relationship between the voltage, current, and charge of the variable capacitor core (not including the series resistance R_s)

$$\begin{aligned} dQ &= C_{\mathrm{var}}dv + vdC_{\mathrm{var}} \\ &= C_0(1 + bv)dv + C_0bvdv \\ &= C_0(1 + 2bv)dv \end{aligned} \tag{3}$$

and

$$dQ = i(t)dt. \tag{4}$$

We then get

$$C_0(1+2bv)\frac{dv}{dt} = i(t). \tag{5}$$

For generality, we assume there are fundamental and second-harmonic voltages across the varactor with independent amplitudes (v_1 and v_2) and relative phase shift θ

$$v(t) = v_1\cos\omega_0 t + v_2\cos(2\omega_0 t+\theta). \tag{6}$$

The harmonics higher than the second are neglected in (6). Such an assumption is valid for a CMOS frequency doubler in the terahertz range. As we will see in Sections IV and V, higher order harmonics are close to or higher than the varactor cutoff frequency, which means the conversions from the fundamental to those harmonics are very weak. If we substitute (6) into (5), the varactor current $i(t)$ is obtained,

$$i(t) = i_{f_0}(t) + i_{2f_0}(t) \tag{7}$$

where i_{f_0} and i_{2f_0} are the fundamental and second-harmonic components of the current

$$i_{f_0}(t) = -\omega_0 C_0 v_1\sin\omega_0 t - \omega_0 C_0 b v_1 v_2\sin(\omega_0 t+\theta) \tag{8}$$

$$i_{2f_0}(t) = -2\omega_0 C_0 v_2\sin(2\omega_0 t+\theta) - \omega_0 C_0 b v_1^2\sin 2\omega_0 t. \tag{9}$$

Having obtained the voltages and currents, we can then derive the fundamental power flow, P_{T,f_0}, into the varactor core

$$\begin{aligned} P_{T,f_0} &= \frac{1}{T_{f_0}}\int_{T_{f_0}}[v_1\cos\omega_0 t\cdot i_{f_0}(t)\cdot dt] \\ &= \frac{1}{2}\omega_0 C_0 b v_1^2 v_2\sin(-\theta). \end{aligned} \tag{10}$$

Similarly, the second-harmonic power, $P_{T,2f_0}$, generated by the varactor core is

$$\begin{aligned} P_{T,2f_0} &= \frac{1}{T_{2f_0}}\int_{T_{2f_0}}[v_2\cos(2\omega_0 t+\theta)\cdot i_{2f_0}(t)\cdot dt] \\ &= -\frac{1}{2}\omega_0 C_0 b v_1^2 v_2\sin(-\theta) \end{aligned} \tag{11}$$

where $P_{T,2f_0}$ is negative to show the varactor is a power source at $2f_0$. It can be seen that the absolute values of the above two powers are equal,

$$P_{T,f_0} = -P_{T,2f_0} = P_T \tag{12}$$

which is as expected because the net power flow of all harmonics in a varactor is zero according to Manley–Rowe principles [33]. P_T in (12) is the power transferred from the fundamental to second harmonic. Up to this point, the varactor is assumed to be lossless. Next, the series resistance, R_s, is included

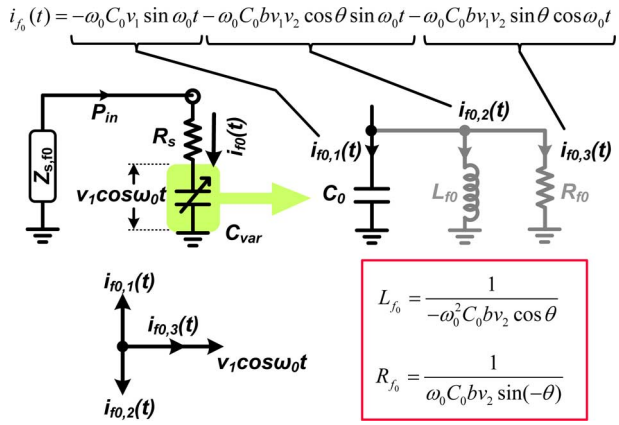


Fig. 4. Three fundamental current components represent an R–L–C network for the impedance of the MOS varactor under power injection at f_0.

to represent the loss, which is the sum of the loss at fundamental and second harmonic

$$\begin{aligned} P_{R_s,f_0} &= \frac{1}{2}|i_{f_0}|^2 R_s \\ &= \frac{1}{2}\omega_0^2 C_0^2 R_s(b^2 v_1^2 v_2^2 + 2b v_1^2 v_2\cos\theta + v_1^2) \end{aligned} \tag{13}$$

$$\begin{aligned} P_{R_s,2f_0} &= \frac{1}{2}|i_{2f_0}|^2 R_s \\ &= \frac{1}{2}\omega_0^2 C_0^2 R_s(4v_2^2 + 4b v_1^2 v_2\cos\theta + b^2 v_1^4). \end{aligned} \tag{14}$$

Using these results, the doubler conversion efficiency η, which is the ratio of the output power at $2f_0$ to the input power at f_0, can be expressed as

$$\begin{aligned} \eta = \frac{P_{\text{out}}}{P_{\text{in}}} &= \frac{P_T - P_{R_s,2f_0}}{P_T + P_{R_s,f_0}} \\ &= \frac{1 - \frac{1}{Q_{2f_0}\sin(-\theta)}\cdot\left(\frac{2v_2}{bv_1^2} + 2\cos\theta + \frac{bv_1^2}{2v_2}\right)}{1 + \frac{1}{Q_{2f_0}\sin(-\theta)}\cdot\left(\frac{bv_2}{2} + \cos\theta + \frac{1}{2bv_2}\right)} \end{aligned} \tag{15}$$

where Q_{2f_0} is the average quality factor of the varactor at $2f_0$

$$Q_{2f_0} = \frac{1}{2\omega_0 C_0 R_s}. \tag{16}$$

The maximum value of v_1 is determined by the linear range of the C–V curve. For varying v_2 and θ, the efficiency in (15) can be optimized analytically or numerically as shown in the design of the 480-GHz doubler in Section IV. By a closer look at (15), we see that for the highest efficiency, the value of θ, the phase shift between the fundamental- and second-harmonic voltages, should be in the third quadrant ($\theta \subset (-180°, -90°)$). Intuitively, this condition leads to a positive transferred power in (10), and smaller loss in (13) and (14).

Next, we derive the source and load impedances, Z_{s,f_0} and $Z_{l,2f_0}$ that achieve the values of v_2 and θ obtained through optimizing (15). The fundamental current, i_{f_0}, can be rearranged into three terms listed in Fig. 4. The first term, $i_{f_0,1}$, leads the input fundamental voltage by 90°, and therefore, represents a capacitor, C_0; this is the same as the small-signal model. However, when θ is between $-180°$ and $-90°$, the second term,

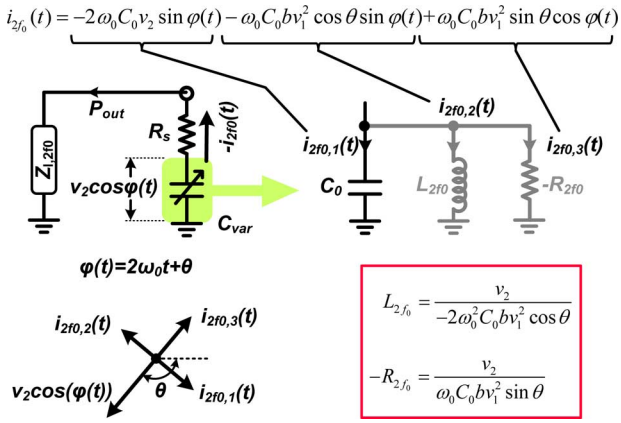


Fig. 5. Three current components at $2f_0$ represent a shunt circuit of C_0, L_{2f_0} and a negative resistance, $-R_{2f_0}$, behaving as a power source at $2f_0$.

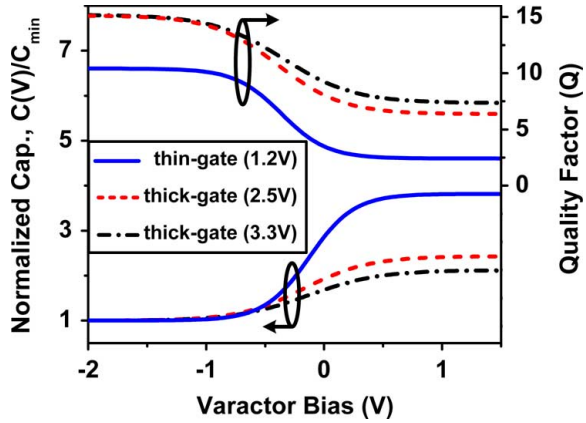


Fig. 6. Simulated capacitance tuning ratios and quality factors (at 100 GHz) of varactors with different gate–oxide thicknesses.

$i_{f_0,2}$, lags the input voltage by 90°, and behaves like an inductor, L_{f_0}. The third term, $i_{f_0,3}$, is even more essential because it is in phase with v_{f_0}, and hence, represents a resistor, R_{f_0}, that absorbs power. In fact, this is the power that is up-converted to $2f_0$, and its value is equal to P_T. Therefore, it is now clear that for the optimum condition, the ring structure should be a match to the entire equivalent circuits in Fig. 4 (including the series R_s) in order to deliver the maximum amount of fundamental input power into R_{f_0}

$$Z_{s,f_0} = Z^*_{\mathrm{var},f_0} = R_s + \frac{1}{Y^*_{\mathrm{core},f_0}}. \tag{17}$$

In (17), Y_{core,f_0} is the input admittance of the varactor core

$$Y_{\mathrm{core},f_0} = \frac{i_{f_0}(s)}{v_1} = sC_0 + \frac{1}{sL_{f_0}} + \frac{1}{R_{f_0}} \tag{18}$$

where $s = j\omega_0$. Similarly, the output admittance of the varactor core at $2f_0$, $Y_{\mathrm{core},2f_0}$, is derived and shown in Fig. 5. It includes a capacitor, C_0, an inductor, L_{2f0}, and a negative resistance, $-R_{2f0}$, as a power source at $2f_0$

$$Y_{\mathrm{core},2f_0} = \frac{i_{2f_0}(s')}{v_2} = s'C_0 + \frac{1}{s'L_{2f_0}} + \frac{1}{-R_{2f_0}} \tag{19}$$

where $s' = 2j\omega_0$. Meanwhile, the series combination of R_s and $Z_{l,2f_0}$ can be obtained,

$$Z_{l,2f_0} + R_s = \frac{v_2}{-i_{2f_0}(s')}. \tag{20}$$

From (19) and (20), we get that at $2f_0$, the ring structure should present the impedance

$$Z_{l,2f_0} = Z^*_{\mathrm{var},2f_0} = -\frac{1}{Y_{\mathrm{core},2f_0}} - R_s \tag{21}$$

to the varactor in order to extract the maximum second-harmonic power out of the device.

IV. Design Case: 480-GHz Passive Doubler

In the previous sections, we introduced device- and circuit-level methods for designing terahertz frequency doublers. In this section, these methods are applied into a practical design of a 480-GHz passive doubler. The choice of the output frequency is due to the limitation of our test setup. The methodology itself is valid for even higher frequency. The 480-GHz doubler is based on the ring topology in Fig. 1, and the design details are described as follows.

A. Optimization of MOS Varactors

In the mainstream CMOS technologies, in addition to the thin gate oxide for fabrication of normal transistors and MOS capacitors, there is also a thick gate–oxide option for 2.5- or 3.3-V I/O circuitries. The 2.5-V-thick gate oxide is used for the varactors of this 480-GHz doubler for the following two reasons.

1) *Power-handling capability*: Varactors with thicker gate oxide can sustain larger voltage swing at the gate, and are therefore more capable for high-power terahertz signal generation. For an output power higher than −10 dBm, the simulated voltage swing across the varactors in this doubler exceeds 2 V. This value is even higher if more output power is needed. This causes reliability issues for thin gate–oxide varactors.
2) *Tradeoff between nonlinearity and loss*: Another advantage of thick oxide varactors is its higher quality factor. The smaller C_{ox} in a thick gate varactor results in lower capacitance density; thus, to achieve a certain capacitance value, a larger active area in shunt is needed, which, in turn, reduces the series resistance R_s. However, the larger proportion of the linear capacitor weakens the nonlinearity. It is shown in [31] that the criterion for varactors in multiplier design is the *dynamic cutoff frequency*, f_c, which is equal to $1/(2\pi C_{\min} R_s) - 1/(2\pi C_{\max} R_s)$. It includes both the loss and nonlinearity of a device. This issue is, however, highly process dependent, thus we simulated all three gate–oxide thickness options in this process, regarding the capacitance tuning ratio and quality factor at 100 GHz (Fig. 6). The f_c of the 2.5-V-thick oxide varactor is 10% higher than the other two (870 GHz versus 790 GHz).

The above simulations are based on varactors with minimum gate length because it gives the highest f_c according to [34]; this is also verified by the simulation in Fig. 7. The varactor that is finally adopted in the design has a gate aspect ratio of

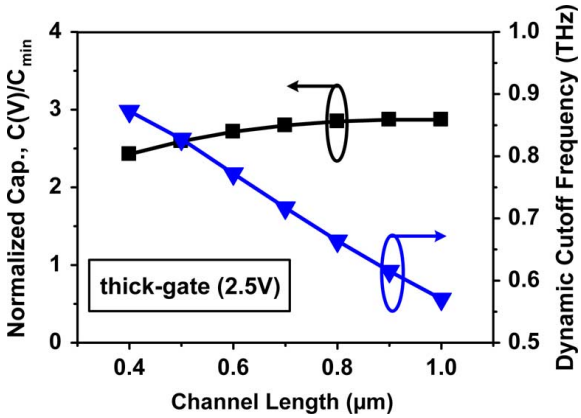


Fig. 7. Simulated capacitance tuning ratios and dynamic cutoff frequency of 2.5-V-thick gate varactors with different gate lengths.

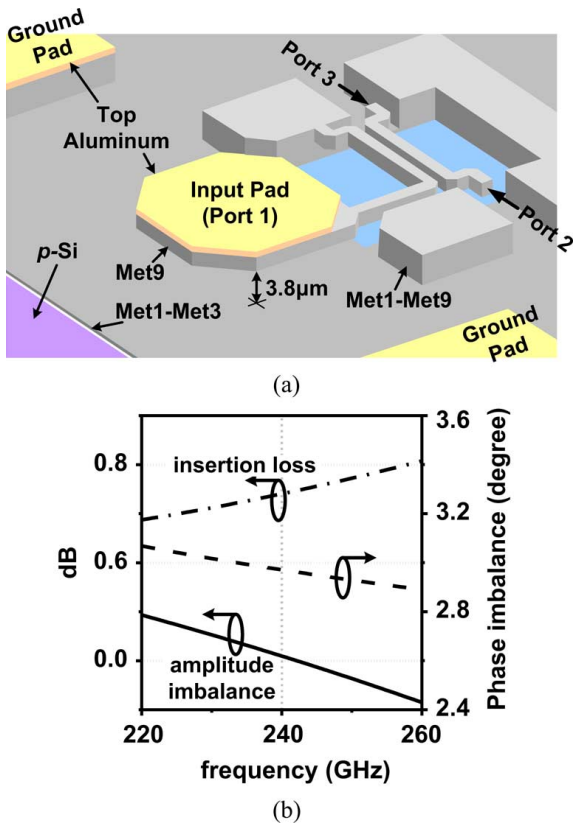


Fig. 8. (a) 3-D structure for the holistic design of the input pad, feed line, and coupled lines in a full-wave simulator. (b) Simulated insertion loss and output imbalance of phase and amplitude.

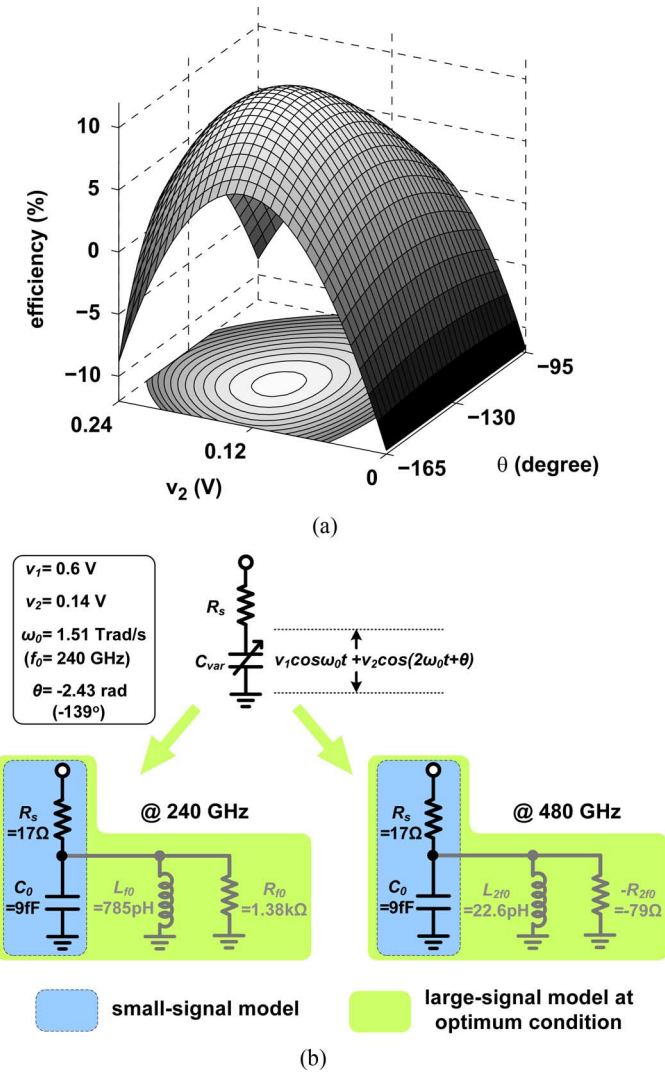


Fig. 9. (a) Calculated conversion efficiency plot using (15) with varying v_2 and θ. The contours enclose the region where efficiency is positive. The step of the contour lines is 1%. (b) Equivalent circuit models of the lossy varactor at 240 and 480 GHz, including the small- and large-signal models at the optimum condition given in (a).

1 μm × 4/0.4 μm, an average capacitance (C_0) of 9 fF, and a series resistance (R_s) of 17.5 Ω.

B. Coupled-Line Structure

To enhance the magnetic coupling field, no ground shield is placed beneath the coupled lines. For lower eddy current induced in the lossy silicon substrate ($\rho \approx 10\ \Omega \cdot$ cm), the width of the coupled lines is small (3 μm) so that the magnetic field is more concentrated near the metal. Narrow lines also reduce the capacitive coupling, which is only 2 fF in simulation, so as to isolate the 480-GHz signals from the input port, as described in Section II. At such high frequencies, the coupled lines are co-designed and simulated with the input ground-shielded pad ($\sim$ 20 fF) and the feed line, in a full-wave EM simulator, HFSS [35]. The simulated even- and odd-mode characteristic impedances are 140 and 25 Ω, respectively. The simulated single-ended to differential insertion loss of the coupled lines at 240 GHz is 0.68 dB [shown in Fig. 8(b)], and the output phase and amplitude imbalance across 40 GHz range are less than 3.1° and 0.2 dB, respectively, which demonstrates a broadband operation capability.

C. Optimum Pumping Conditions

In Section IV-B, the first-order approximated efficiency expression is derived in (15). For the varactor used in this 480-GHz doubler, the fundamental voltage amplitude, v_1 is about 0.6 V, the quality factor at 480 GHz is 2.1, and the linearized C–V curve slope, b, is 0.57 V^{-1}. Based on these, the efficiency for varying values of v_2 and θ is plotted in Fig. 9(a). In the case of

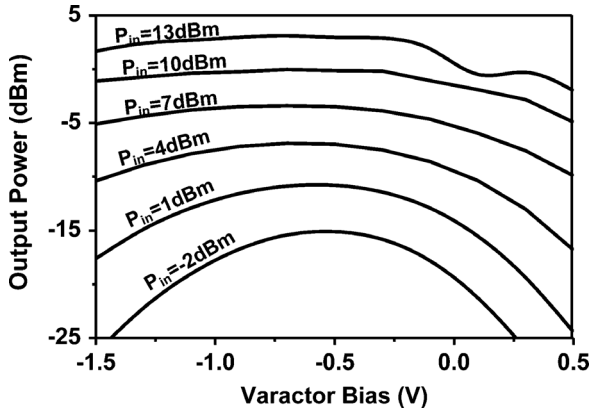


Fig. 10. Simulated output power contour of a varactor with varying input power levels ($f_0 = 240$ GHz) and gate bias voltages, under the optimum pumping/loading conditions.

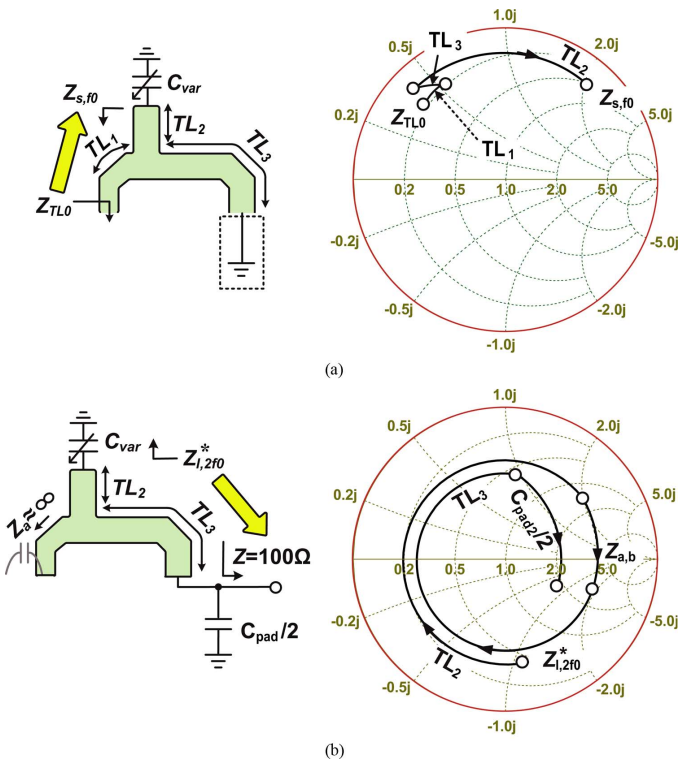


Fig. 11. Half-circuit analysis of the matching scenario and the simulated impedance transformation shown on a Smith chart ($Z_0 = 39\ \Omega$) at: (a) $f_0 = 240$ GHz and (b) $f_0 = 480$ GHz.

TABLE I
DIMENSIONS OF THE 480-GHz DOUBLER RING

	TL_0	TL_1	TL_2	TL_3
Length (μm)	27	7	92	110

a frequency doubler, the *passive* load impedance of the varactor at $2f_0$ is associated with the *positive* efficiency region of the surface. It can be seen that the peak efficiency of 11.4% occurs when v_2 is 0.14 V and θ is $-139°$. Under such optimum condition, the large-signal model parameters are derived in Fig. 9(b) according to the equations in Figs. 4 and 5. Though R_{f_0} is large compared to the impedance of C_0 at 240 GHz, it is not trivial

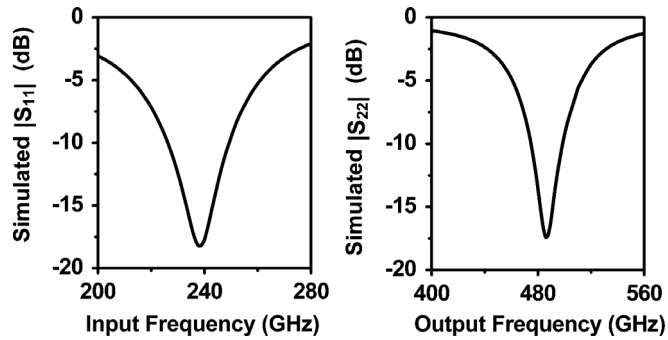


Fig. 12. Large-signal S-parameter simulations of the entire 480-GHz frequency doubler. The input stimulus power level is 4.5 dBm.

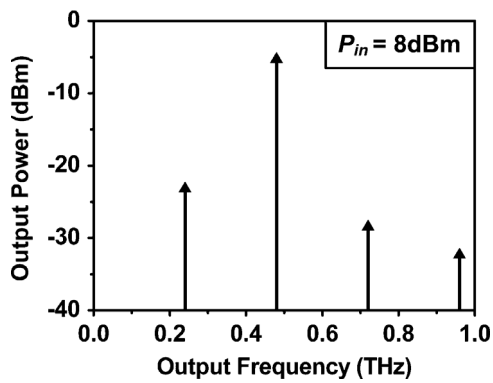


Fig. 13. Simulated output power at fundamental, second, third, and fourth harmonics.

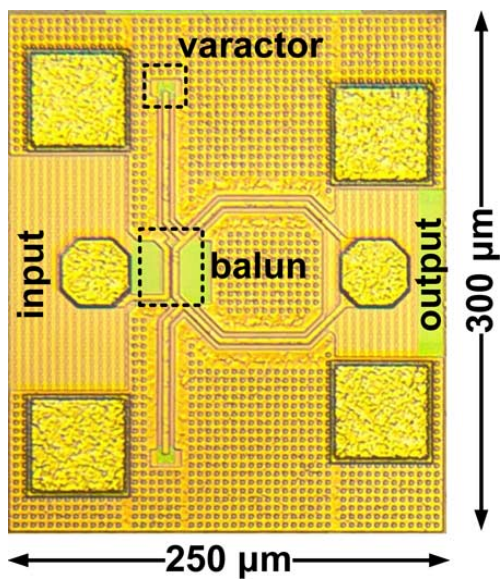
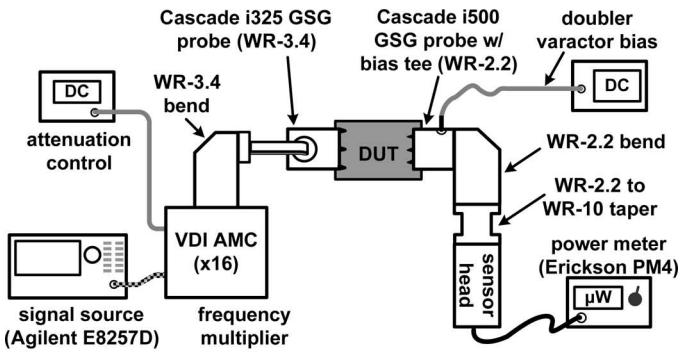


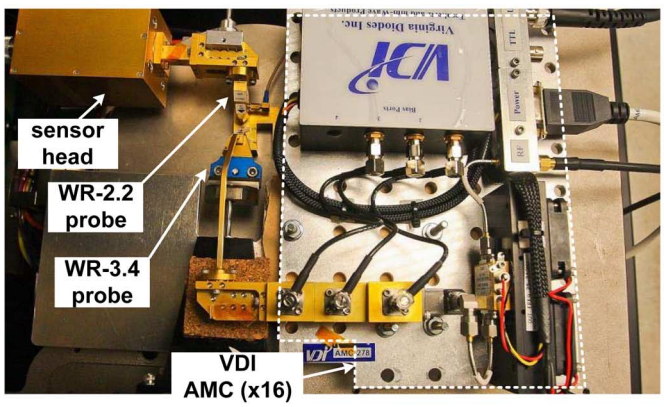
Fig. 14. Microphotograph of the 480-GHz CMOS frequency doubler.

because only the fundamental power absorbed into R_{f_0} is up converted. Based on (17) and (21), the optimum source and load impedances, Z_{s,f_0} and $Z_{l,2f_0}$, are $(22+78j)\Omega$ and $(23+40j)\Omega$. When the varactor is terminated by these impedances, its output power at $2f_0$ is simulated by Agilent ADS [36] with different input power levels and bias voltages (Fig. 10). It can be seen that the simulated peak efficiency is 10%, which is close to the calculated result.



Loss at 240 GHz		Loss at 480 GHz	
Cascade i325 probe	5.5 dB	Cascade i500 probe	8 dB
WR-3.4 bend	1.5 dB	WR-2.2 bend	2 dB
		WR-2.2 to WR-10 taper	1 dB

(a)



(b)

Fig. 15. (a) Block diagram and (b) photograph of the testing set up for the 480-GHz frequency doubler.

D. Matching Implementations in the Ring Structure

Next, the ring structure is designed to present Z_{s,f_0} to the varactor at f_0, and to transform $Z_{\mathrm{var},2f_0} = Z^*_{l,2f_0}$ to 100 Ω at $2f_0$ so that the doubler output can match to 50 Ω with two-branch combining. The input matching scenario is presented in Fig. 11(a). Due to the symmetry of the ring, only the half circuit is analyzed with a virtual ground on the right. As discussed in Section II, the signal at f_0 is more sensitive to the left half of the ring, as well as the input pad and feed line. Therefore, the length of TL_3 is designed to be close to a quarter-wavelength so that it acts as a large shunt inductor and does not significantly affect the input matching. Similarly, the output matching scenario is presented in Fig. 11(b). The signal at $2f_0$ is more sensitive to the right half of the ring, as well as the output pad, so TL_1 is made short, to reduce the parasitic shunt capacitance of the left half of the ring. The lengths of the transmission lines are listed in Table I. Due to the close proximity (3.8 μm) between the signal and ground metal, the characteristic impedance of $\mathrm{TL}_1 \sim \mathrm{TL}_3$ is only 39 Ω. At 240 GHz, the HFSS simulated attenuation factor of the transmission line is 1.6 dB/mm. The capacitances of the input/output ground-shielded pads are also included in the matching design.

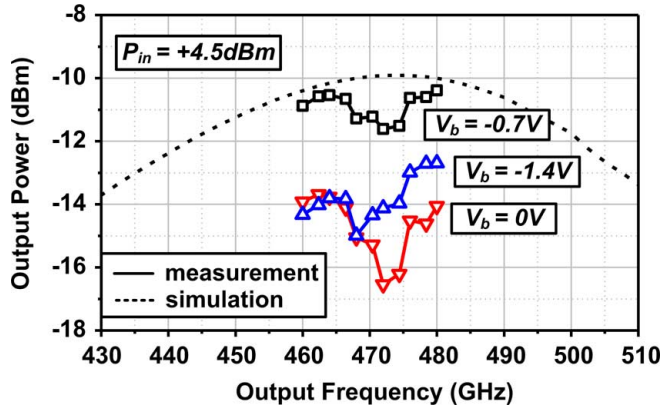


Fig. 16. Output power contour of a varactor with varying input power levels ($f_0 = 240$ GHz) and gate bias voltages under the optimum pumping conditions.

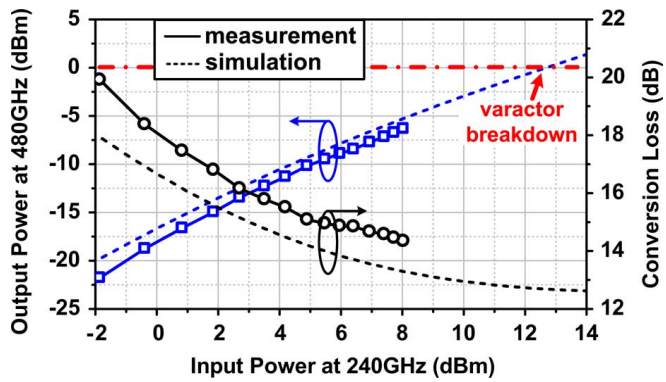


Fig. 17. Measurement and simulation results of the output power and conversion loss of the doubler at different input power levels at 240 GHz.

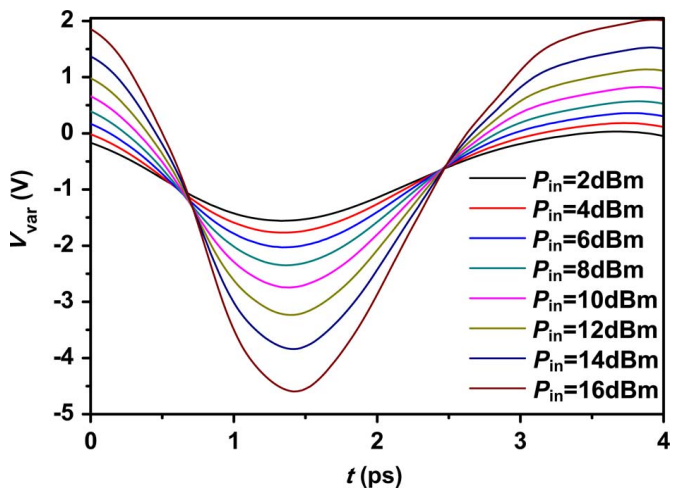


Fig. 18. Simulated waveforms of the voltage across the varactor in the doubler at different input power levels at 240 GHz.

E. Simulated Performance

To accurately model the ring, the whole metal structure, including the input/output ground–signal–ground (GSG) pads and the lossy substrate, is simulated up to the fourth harmonic using HFSS. The matching performance of the entire doubler is verified using the large-signal S-parameter simulation (shown in Fig. 12). It can be seen that this compact ring structure

TABLE II
COMPARISON OF STATE-OF-THE-ART TERAHERTZ SIGNAL SOURCES IN SILICON

References	[22]	[23]	[8]	[19]	[16]	[40]	[26]	This Work
f_{out} **(GHz)**	275	325	180	290	482	533	125	480
Source Type	active doubler			harmonic oscillator			passive doubler	
Conversion Loss (dB)	11.4	6 (gain)	6.4	0	0	0	10	14.3
$P_{out,max}$ **(dBm)**	-6.6	-3	0	-1.2	-7.9	-36	-1.5	-6.3
3-dB Output Bandwidth	7.8%	6.3%	11.1%	4.5%	0	0.1%	N/A	†14.6% (sim)
DC Power (mW)	40	24	39	325	61	64	0	0
Technology	65-nm CMOS	130-nm SiGe	45-nm CMOS	65-nm CMOS	65-nm CMOS	45-nm CMOS	130-nm CMOS	65-nm CMOS

† The full 3-dB bandwidth could not be measured due to the limited input source bandwidth (10 GHz).

achieves reasonable input matching at f_0 and output matching at $2f_0$. Meanwhile, due to the simplicity of the ring and the broadband characteristics of the coupled-line balun, the reflection coefficients stay low within a wide frequency range. When driven by an input power of 8 dBm at 240 GHz, the doubler output power at fundamental, second, third, and fourth harmonics is also simulated in Fig. 13. The second-harmonic power is 18-dB higher than the fundamental power at the output, indicating that an effective signal filtering is achieved by the ring structure. Other simulation results will be given in Section V for comparison with the measurement.

V. EXPERIMENTAL RESULTS

The 480-GHz doubler was fabricated using 65-nm LP bulk CMOS technology, and the chip micrograph is shown in Fig. 14. The doubler, including the input/output GSG pads, occupies an area of only 300 × 250 μm^2. To test the chip, a VDI amplifier multiplier chain (AMC) is used to feed the 240-GHz input signal through a Cascade i325 WR-3.4 probe [see Fig. 15(a)]. The input signal power at different frequencies and user-control levels is calibrated by an Erickson PM4 power meter. On the output side, the 480-GHz signal is extracted through a Cascade i500 WR-2.2 probe, and is then delivered into the power meter for measurement. The losses of the probes and waveguides at 240 and 480 GHz are listed in Fig. 15(a) [37], [38]. The output probe has an integrated bias tee, which can provide a bias voltage through the ring structure to the varactors gate. The bias current is only about 50 μA due to the discharging resistors, R_{p1} and R_{p2}. A photograph of the testing set up is shown in Fig. 15(b), in which all the components are connected using rigid waveguides. The following two reasons validate that the measured power from the power meter comes from the second-order component rather than fundamental and higher harmonics: 1) for the WR-2.2 waveguide at the output side, the cutoff frequency for the lowest propagation mode, TE_{10}, is 268 GHz [38], which means that any possible fundamental-frequency power leakage to the output cannot be delivered to the power meter; 2) the simulated third- and fourth-harmonic power at the output (shown in Fig. 13) are over 20 dB lower than the second harmonic; 3) the tip of the output probe, which

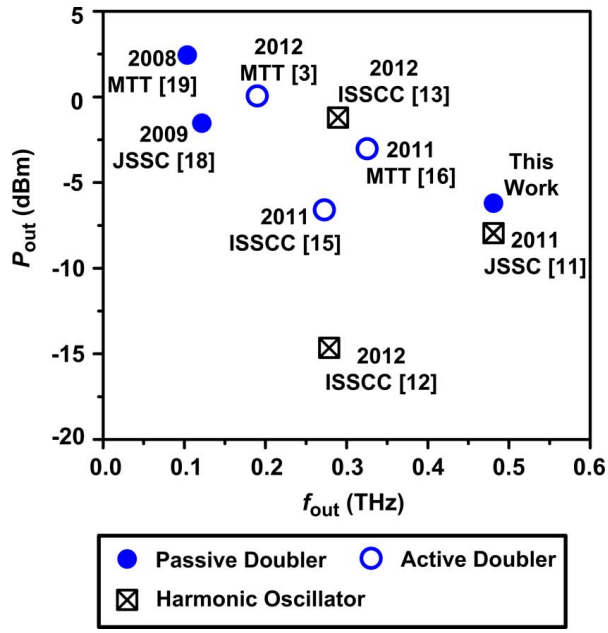


Fig. 19. State-of-the-art terahertz sources in silicon: output power versus frequency. The merit in [17] is the power from each DAR element out of the 16-element array for fair comparison.

is based on a coplanar waveguide (CPW) structure, is expected to have significant loss at 720 and 960 GHz.

Using the user-control port of the VDI AMC, the de-embedded source power is fixed at 4.5 dBm, while the source frequency is swept. The measured output power of the doubler is plotted in Fig. 16 with different varactor bias voltages. Consistent with the simulations in Fig. 10, the optimum bias voltage in measurement is -0.7 V, and it can be seen that the measured output power level is close to the simulation. Unfortunately, the safety operational frequency range of the source is only from 230 to 240 GHz, which we believe is much smaller than the bandwidth of the doubler. This makes sense as the measured output power has only 1.5-dB fluctuation and does not show any roll-off tendency within the 20-GHz range of measurement. Actually, as Fig. 16 shows, the simulated 3-dB output bandwidth of this doubler is as high as 70 GHz. The $\sim$2-dB dips in the

measured curves in Fig. 16 may due to the small discrepancy between the characterized and the actual losses of the probes and waveguides, and due to the small internal reflections among these components.

Next, at the input frequency of 240 GHz, the power injected into the chip is changed from -2 dBm to the highest 8 dBm. The measured doubler output response is plotted in Fig. 17. The maximum (but unsaturated) output power is as high as -6.3 dBm (0.23 mW). In Fig. 17, the simulated output power reaches 2 dBm without saturation. However, the maximum output power is limited by the breakdown voltage of the MOS varactors. Therefore, the waveforms of the voltage across the varactor with different doubler input power levels are simulated in Fig. 18. In this CMOS process, the 2.5-V device can be overdriven to 3.3 V [39]. Thus, based on Figs. 17 and 18, the maximum output power is expected to be 0 dBm if higher input power is available in the measurement. Fig. 17 also indicates that, with larger input power, the conversion loss of the doubler keeps decreasing and reaches a measured minimum of 14.3 dB.

VI. Conclusions

In this paper, we introduced a ring structure and an analytical optimization method for the design of a varactor-based frequency doubler in the terahertz range. Based on these, a 480-GHz CMOS doubler is designed and measured. In Table II, the performance of the doubler is compared to the state-of-the-art sub-millimeter-wave/terahertz signal sources. To the best of our knowledge, our 480-GHz doubler provides the highest output frequency among all the CMOS frequency multipliers, and the highest output power in all CMOS signal sources above 350 GHz, including harmonic oscillators. Regarding different power levels generated at different frequencies, the performance of the state-of-the-art silicon signal sources are plotted in Fig. 19. It can be seen that these sources also follow the trend of *terahertz gap* [14], and this work has a good standing in such a trend.

Acknowledgment

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Ruonan Han (S'10) was born in Hohhot, China, in 1984. He received the B.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2007, the M.Sc. degree in electrical engineering from the University of Florida, Gainesville, FL, USA, in 2009, and is currently working toward the Ph.D. degree in electrical engineering at Cornell University, Ithaca, NY. His doctoral research is focused on terahertz signal generation and detection circuits using CMOS and GaN technologies. His completed projects include a 260-GHz radiator array based on harmonic oscillators, a 480-GHz passive frequency multiplier, and a 280-/860-GHz Schottky diode image sensor.

In the summer of 2012, he was an Intern with Rambus Inc., Sunnyvale, CA, USA, where he was involved with fast-locking clock and data recovery circuits. He has authored or coauthored over 20 journal and conference publications.

Mr. Han is a student member of the IEEE Solid-State Circuits Society. He is a reviewer for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and the IEEE International Symposium on Circuits and Systems (ISCAS). He was the recipient of the Best Student Paper Award (2nd Place) of the 2012 Radio-Frequency Integrated Circuits (RFIC) Symposium and the Helic Student Scholarship of the 2010 Custom Integrated Circuits Conference (CICC). He was also the recipient of the Irwin and Joan Jacobs Fellowship (2011), the John M. Olin Fellowship (2010), and the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award (2012–2013).

Ehsan Afshari (S'98–M'07–SM'11) was born in 1979. He received the B.Sc. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, in 2001, and the M.S. and Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 2003 and 2006, respectively.

In August 2006, he joined the faculty of the Department of Electrical and Computer Engineering, Cornell University, Ithaca, NY. His research interests are millimeter-wave and terahertz electronics and low-noise integrated circuits for applications in communication systems, sensing, and biomedical devices.

Prof. Afshari is the chair of the IEEE Ithaca Section and chair of Cornell Highly Integrated Physical Systems (CHIPS). He is a member of the International Technical Committee, IEEE Solid-State Circuit Conference (ISSCC), the Analog Signal Processing Technical Committee, IEEE Circuits and Systems Society, the Technical Program Committee, IEEE Custom Integrated Circuits Conference (CICC), and the Technical Program Committee, IEEE International Conference on Ultra-Wideband (ICUWB). He was the recipient of the National Science Foundation CAREER Award (2010), Cornell College of Engineering Michael Tien Excellence in Teaching Award (2010), Defense Advanced Research Projects Agency (DARPA) Young Faculty Award (2008), and Iran's Best Engineering Student Award presented by the President of Iran (2001). He was also the recipient of the Best Paper Award of the Custom Integrated Circuits Conference (CICC) (2003), First Place of the Stanford-Berkeley-Caltech Inventors Challenge (2005), the Best Undergraduate Paper Award of the Iranian Conference on Electrical Engineering (1999), the Silver Medal of the Physics Olympiad (1997), and the Award of Excellence in Engineering Education from the Association of Professors and Scholars of Iranian Heritage (APSIH) (2004).