15.4 A 283-to-296GHz VCO with 0.76mW Peak Output Power in 65nm CMOS

Yahya M. Tousi, Omeed Momeni, Ehsan Afshari

Cornell University, Ithaca, NY

Sub-mm-Wave and terahertz frequencies have many applications such as medical imaging, spectroscopy and communication systems. CMOS signal generation at this frequency range is a major challenge due to the limited cut-off frequency of transistors and their low breakdown voltage. A recent work has demonstrated generation of high power at a fixed frequency in the sub-mm-Wave range using a harmonic oscillator [1]. However, for most applications a tunable signal source is necessary. In previous works, frequency multipliers are used as an alternative for tunable power generation above 150GHz [2]. In this work, for the first time we introduce a tunable high-power oscillator at sub-mm-Wave frequencies in low-power (LP) bulk CMOS.

There is a tradeoff between power generation and tuning range in high-frequency VCOs. This is primarily because the quality factor of tuning varactors decreases rapidly with frequency. Therefore, tuning frequency with varactors results in significant drop of output power. Because of this tradeoff, the best reported CMOS VCOs above 150GHz generate sub-μW output power even though they have <2% tuning range. To achieve both high output power and tuning capability at sub-mm-Wave frequencies, we exploit a novel architecture that decouples power generation from frequency tuning.

The proposed architecture shown in Fig. 15.4.1 consists of a loop of coupled oscillators. In this scheme, each oscillating core couples energy to its neighbor through a tunable phase shifter. The phase shifters adjust the coupling between cores and as explained below, control the frequency of core oscillators. Since the frequency tuning is performed by controlling the coupling, the core oscillators are varactor-free and hence can be optimized for maximum power generation at the desired harmonic frequency. By adjusting the loop dynamics, we ensure that the desired harmonics from all core oscillators are in phase and combined at the output node.

The tuning method is inspired by injection locking between two oscillators: when an oscillator at ω injects enough energy to another oscillator with a free running frequency of ω_0, within locking range, the second oscillator locks to ω. As shown in Fig. 15.4.2, in the locked mode, a phase lag $\Delta\varphi$ is developed between the locked oscillator and the injecting source which is proportional to ω-ω_0 and inversely proportional to the coupled energy [3]. We exploit an interesting implication of this concept. By adjusting the phase shift $\Delta\varphi$ between the two oscillators, we concurrently control the frequency of both of them. To realize this idea, we place the oscillators in a loop configuration with phase shifters (ψ) between neighbors as shown in Fig. 15.4.2. It can be shown that the loop with N oscillators has N different coupling modes corresponding to a phase difference of $2k\pi/N$ between adjacent oscillators where k=0 to N-1. By properly selecting the range of ψ, we can select a desired mode and damp the rest.

The phase difference between oscillator cores is fixed and depends on the coupling mode. This constant phase shift is the sum of two variable phase shifts. The first part, ψ which is set by the phase shifter, is the phase difference between the preceding oscillator and the actual injected signal V_{inj}. The second part, $\Delta\varphi$, is the phase shift between the injected signal V_{inj} and the succeeding oscillator. In this setting all oscillators are locked to the same frequency that is set by $\Delta\varphi$ which is forced by ψ and the coupling mode. The frequency tuning range is proportional to the injected power and inversely proportional to the quality factor of the tank as shown in Fig. 15.4.2.

In this work, we design a loop with four coupled oscillators. This corresponds to four coupling modes and we select the mode with $\pi/2$ phase shift between adjacent core oscillators. This results in constructive combining at the fourth harmonic of the fundamental frequency and cancellation of lower harmonics as shown in Fig. 15.4.3. We carefully select the fourth harmonic to maximize the power around 300GHz. A higher harmonic number results in smaller nonlinearity and hence lower output power. A lower harmonic number makes the fundamental frequency too close to f_{max} (~200GHz) resulting in smaller swing and hence weaker harmonics.

The phase shifter is a two-stage differential amplifier shown in Fig. 15.4.1. The supply node of each stage is virtual ground and is wirebonded off the chip. The phase shift is controlled by adjusting the varactors through $V_{control}$. The varactors are buffered from the oscillator through M_1 and do not affect the power generation at the core. The highest amount of phase tuning is possible around the resonance frequency of the load of amplifiers. This frequency is designed to be at the resonance frequency of the tank of core oscillators resulting in the maximum frequency tuning.

To deliver high harmonic power to the load, it is essential to generate strong harmonics at each core oscillator and effectively transfer it to the output. Figure 15.4.3 shows the equivalent half circuit of each core at the fourth harmonic. The gate inductance L_g partially resonates with the gate capacitance of the device, resulting in higher swing at the fundamental and hence stronger harmonic generation. More importantly, L_g provides a local matching between the drain impedance Z_{drain} and the combiner network impedance Z_{out} as shown in the Smith chart of Fig. 15.4.3. This guarantees that most of the generated harmonic flows to the load and does not go back to the gate of the transistor. The next matching is performed at the output of the power combiner. This matching network, which includes the output pad, is also designed at the fourth harmonic. Metal walls and ground shielding are used for the cores and the power combiner to avoid cross coupling between adjacent blocks.

The VCO is fabricated in a 65nm LP bulk CMOS process. Figure 15.4.4 shows the test setup to measure the output frequency and power. The output is measured using a Cascade i325-GSG probe with a built-in bias tee. Frequency measurement is performed by connecting the probe to a VDI WR-3.4EHM harmonic mixer. The detected output frequency and harmonic number of the LO are found by sweeping the LO and observing the IF. Figure 15.4.4 shows a typical IF spectrum mixed with the 16th harmonic of the LO. Two versions of the chip with different drain inductances (L_d in Fig. 15.4.1) are measured with center frequencies of 290GHz and 320GHz and respective tuning ranges of 13GHz and 8.4GHz shown in Fig. 15.4.5. At 323GHz, the measured phase noise of the oscillator is -77dBc/Hz at 1MHz offset frequency. The output power is measured using an Erikson PM4 power meter as illustrated in Fig. 15.4.4. The losses of the probe and all the other components in this setup are calibrated using a 500GHz network analyzer. The power testing setup uses WR3.4 waveguides that filter the fundamental and second harmonic. The third harmonic power is suppressed by the output power combining network and hence its power at the output is at least 15dB lower than the fourth harmonic. This is verified by observing the output spectrum using the mixer. Measurement results in Fig. 15.4.5 show the output power as a function of DC power and control voltage. A peak output power of -1.2dBm is measured at 292GHz. Figure 15.4.6 shows the comparison with prior art. This work demonstrates the highest output power and tuning range among the CMOS VCOs in this range and is comparable with sources in compound semiconductors with much higher f_{max}.

Acknowledgment:
The authors acknowledge the TSMC University Shuttle Program for chip fabrication, Sonnet for software support and the support of the C2S2 Focus Center under the FCRP, an SRC entity, and the National Science Foundation.

References:
[1] O. Momeni, and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–297, Mar. 2011.
[2] B. Cetinoneri *et al.*, "W-Band Amplifiers with 6 dB Noise Figure and mW-Level 170-200 GHz Doublers in 45-nm CMOS", *IEEE Trans. Microwave Theory and Techniques*, vol. 60, no. 1, Jan. 2012.
[3] R. Adler, "A Study of Locking Phenomena in Oscillator," *Proc. IRE*, vol. 34, pp. 351–357, June 1946.
[4] D. Huang *et al.*, "324GHz CMOS Frequency Generator Using Linear Superposition Technique," *ISSCC Dig. Tech. Papers*, pp. 476–477, Feb. 2008.
[5] K. Sengupta, and A. Hajimiri, "Distributed Active Radiation for THz Signal Generation," *ISSCC Dig. Tech. Papers*, pp. 288–289, Feb. 2011.
[6] M. Seo *et al.*, "InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz", *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2203–2214 Oct. 2011.
[7] E. Öjefors, B. Heinemann, and U. R. Pfeiffer, "Active 220- and 325-GHz Frequency Multiplier Chains in an SiGe HBT Technology," *IEEE Trans. Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1311-1318, May 2011.

 978-1-4673-0377-4/12/$31.00

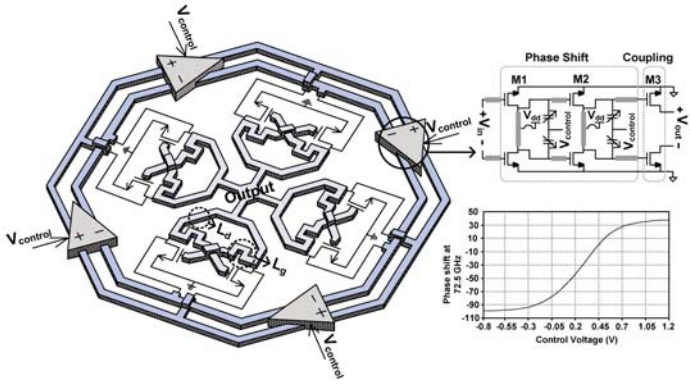

Figure 15.4.1: The VCO consisting of four coupled oscillators. Right: The phase shifter and its simulated phase shift as a function of the control voltage at the fundamental frequency.

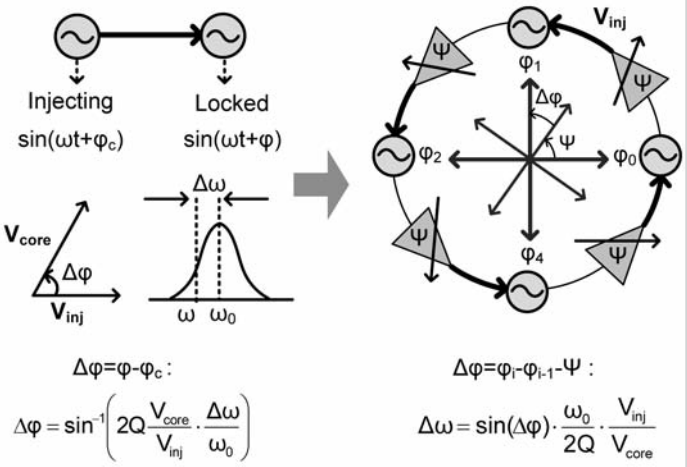

Figure 15.4.2: Left: Phase shift as a result of injection locking. Right: The inverse effect resulting in frequency change in coupled oscillators.

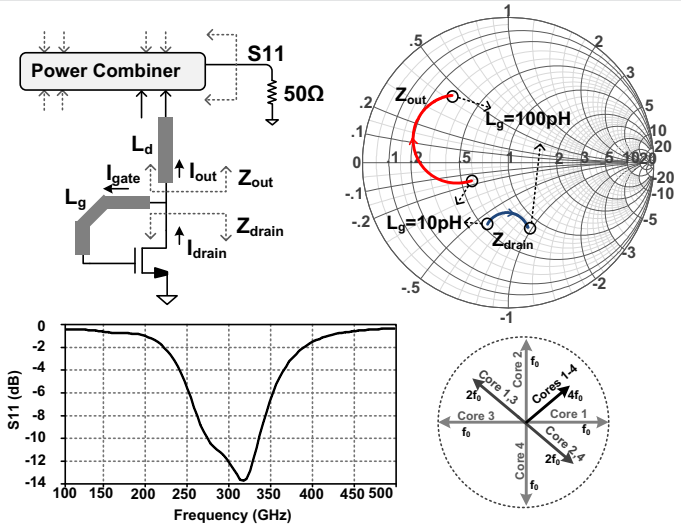

Figure 15.4.3: Top: Local matching at the harmonic by adjusting L_g. Bottom: Output matching and cancellation of lower harmonics.

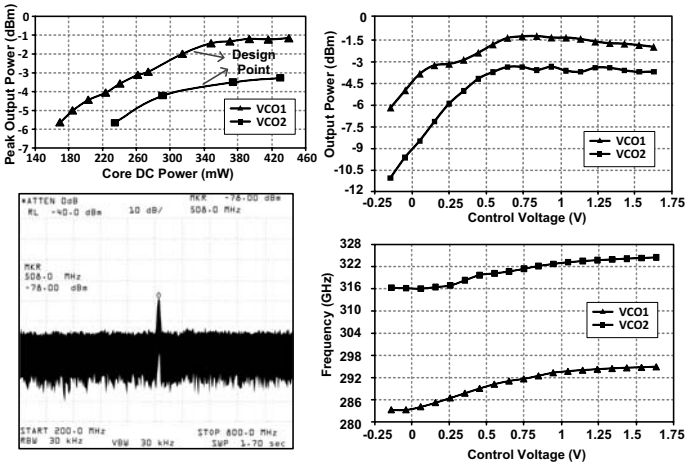

Figure 15.4.4: Measured peak output power and a typical IF spectrum after mixing with the 16th harmonic of LO=18.452GHz. Right: Measured output power and frequency at the indicated design points.

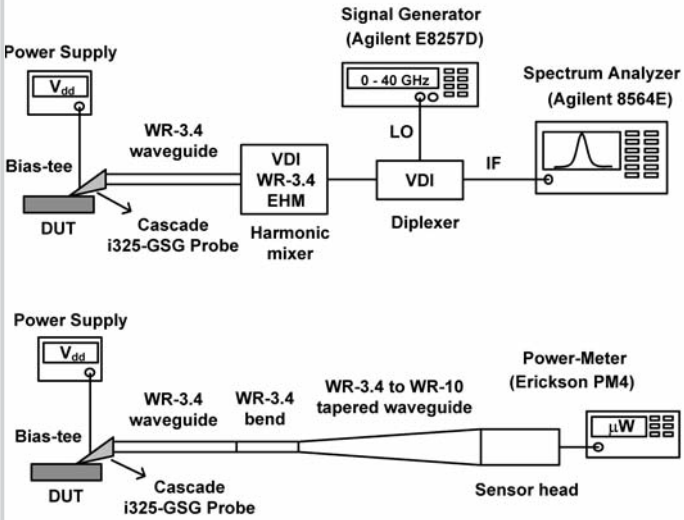

Figure 15.4.5: Measurement setup used for frequency (top) and power (bottom) measurements.

Ref.	This work	This work	[1]	[4]	[5]	[6]	[2]*	[7]*
Frequency (GHz)	290	320	482	324	291	296	190	325
Output Power (dBm)	-1.2	-3.3	-7.9	-46	-10.9 (radiated, 4 elements)	-3.9	0	-3
Tuning Range	4.5%	2.6%	Not tunable	1.2%	Not tunable	4%	13.6%	6.2%
Phase Noise (dBc/Hz)	-78 @ 1 MHz	-77 @ 1 MHz	-76 @ 1 MHz	-78 @ 1 MHz	NA	-78 @ 1 MHz	NA	-101 @ 1 MHz**
DC Power (mW)	325	339	61	12	74	115	91	420
Technology	65nm LP bulk CMOS	65nm LP bulk CMOS	65nm bulk CMOS	90nm bulk CMOS	45nm SOI CMOS	InP HBT (f_{max}>800 GHz)	45nm SOI CMOS	130nm SiGe HBT
Area (mm^2)	0.36	0.36	0.02	0.03	0.64	0.41	0.56	0.51

* [2] and [7] are frequency multipliers, not oscillators. We added these works to the table to compare with frequency multipliers at similar frequencies.
** Driven by a low phase noise source. This level of source phase noise is not achievable on silicon.

Figure 15.4.6: Comparison with the state-of-the-art signal sources above 180GHz.

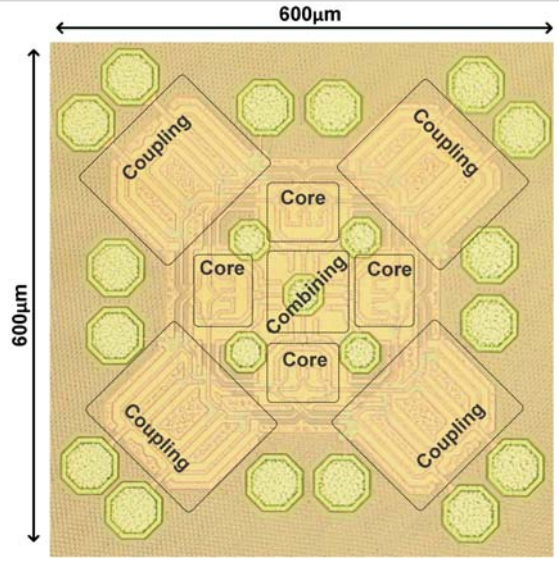

Figure 15.4.7: Chip micrograph.

978-1-4673-0377-4/12/$31.00