High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach

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***Abstract*—A systematic approach to designing high frequency and high power oscillators using activity condition is introduced. This method finds the best topology to achieve frequencies close to the $f_{\max}$ of the transistors. It also determines the maximum frequency of oscillation for a fixed circuit topology, considering the quality factor of the passive components. Using this technique, in a 0.13 μm CMOS process, we design and implement 121 GHz and 104 GHz fundamental oscillators with the output power of -3.5 dBm and -2.7 dBm, respectively. Next, we introduce a novel triple-push structure to realize 256 GHz and 482 GHz oscillators. The 256 GHz oscillator was implemented in a 0.13 μm CMOS process and the output power of -17 dBm was measured. The 482 GHz oscillator generates -7.9 dBm (0.16 mW) in a 65 nm CMOS process.**

***Index Terms*—Activity condition, CMOS, harmonic generation, maximum oscillation frequency, millimeter-wave, oscillator, ring oscillator, sub-millimeter wave, terahertz, triple-push.**

I. INTRODUCTION

THERE is growing interest in signal generation in the millimeter-wave and terahertz frequency ranges [1], [2]. There are numerous applications for mm-wave frequencies such as broadband wireless access (e.g., WiMax), vehicular radar, short-range communication, and ultra-narrow pulse generation for UWB radar [3], [4]. Imaging and bio/molecular spectroscopy were the first and the main applications of the terahertz band, which is usually defined to be between 300 GHz and 3 THz [5]–[8]. Recently, this range has also been used for high data rate communication, compact range radar, and remote sensing [8]–[11].

Signal generation at these frequencies is a major challenge in solid-state electronics due to the limited cut-off frequency and breakdown voltage of active devices as well as the lower quality factor of passive components caused by ohmic and substrate loss. Traditionally, compound semiconductors are used to implement fundamental oscillators at mm-wave and terahertz frequencies [12]–[16]. Recently, SiGe and CMOS transistors were also employed to generate signals in the same frequency range using fundamental and push-push oscillators [17]–[26]. A fundamental oscillation frequency of 346 GHz is achieved in [13] using a 35 nm InP HEMT with a maximum oscillation frequency ($f_{\max}$) of 600 GHz. SiGe HBTs with an $f_{\max}$ of 160 GHz are used in [24] to achieve a fundamental oscillation frequency of 100 GHz. A 104 GHz fundamental oscillator is also reported in [22], which employs 90 nm CMOS transistors with an $f_{\max}$ of 300 GHz. In all of these oscillators, the oscillation frequency is around half of the $f_{\max}$ of the transistors. The question that arises is whether the oscillators have exploited the full capacity of the active devices in terms of output power and frequency. In other words, in any given process, it is essential to find the maximum oscillation frequency of a circuit topology, considering the quality factor of the passive components. Furthermore, for a fixed frequency, it is important to determine the topology that results in maximum output power.

In this paper, we address the above questions by investigating the effect of oscillator topology and the quality factor of the passive components on the oscillation frequency using the *activity condition* of the transistors [27]. We then introduce a methodology to design oscillators with frequencies close to the $f_{\max}$ of the transistors. Using this methodology in a 0.13 μm CMOS process with $f_{\max}$ of around 135 GHz [28], we design and implement 121 GHz and 104 GHz oscillators with the output power of -3.5 dBm and -2.7 dBm, respectively. Triple-push oscillators have been used to effectively generate third harmonics of the fundamental frequency [29], [30]. In this work, we introduce and realize a novel triple-push oscillator at 256 GHz with an output power of -17 dBm in the same 0.13 μm CMOS process. Next, using the same topology we implement a 482 GHz oscillator with a measured output power of -7.9 dBm in a 65 nm CMOS process. To the best of our knowledge, the 121 GHz and the 104 GHz oscillators have the highest power among CMOS oscillators in this frequency range, and the 121 GHz oscillator has the highest fundamental frequency in a 0.13 μm CMOS process. The 256 GHz oscillator has the highest frequency in a 0.13 μm CMOS process. The 482 GHz oscillator has the highest reported power in any CMOS or SiGe process and is comparable with InP HEMT and InP HBT in this frequency range.

The rest of this paper is organized as follows. In Section II, the origin of $f_{\max}$ and the activity condition of a two-port active device are discussed. In Section III, we extend the theory of Section II for oscillators and use it to introduce a method for designing high frequency oscillators. The design, simulation and measurement of the 121 GHz and 104 GHz oscillators are discussed in Section IV. The two triple-push oscillators at 256 GHz and 482 GHz, along with the simulation and measurement results are presented in Section V. Finally, we summarize the paper in Section VI.

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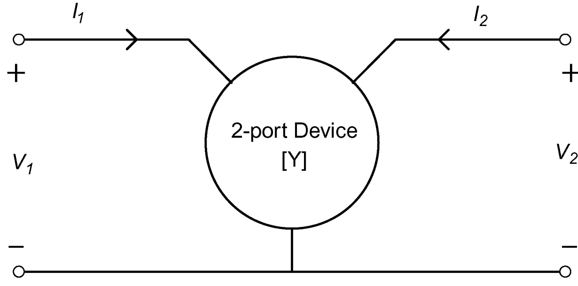


Fig. 1. A three-terminal two-port device.

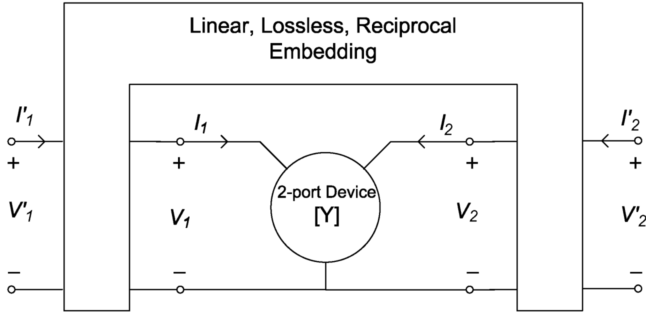


Fig. 2. A device embedded in a 4-port, linear, lossless, reciprocal network.

II. Overview of the Activity Condition of a Two-Port Device

Activity condition determines the criterion in which the device can generate power. This is the basis for defining the maximum oscillation frequency, $f_{\max}$. Before discussing the activity of a device, it is useful to understand Mason's invariant, U.

A. Unilateral Power Gain and the Origin of $f_{\max}$

In 1954, Mason introduced the invariant function U for a linear two-port network [31]. For a three-terminal device as a linear two-port network shown in Fig. 1, U is defined as

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{12}G_{21})} \tag{1}$$

in which Y_{ij}'s are the elements of the admittance matrix of the network, $G_{ij} = \mathrm{Real}[Y_{ij}]$, and $i, j = 1, 2$. The intriguing property of U is that it is invariant under any 4-port, linear, lossless, reciprocal embedding shown in Fig. 2 [32]. The resulting embedded device is described by the admittance matrix, Y'. In other words for any two-port device such as a transistor, U is only a function of the inherent characteristics of the device and not the embedding components. The fact that U is invariant under any linear, lossless, reciprocal embedding also implies that it does not change with respect to the node connections. For example, in a FET device, if we connect gate, source, and drain nodes to any of the three terminals of Fig. 1, the value of U remains the same. Besides being invariant, Mason showed that U is the maximum power gain when the reverse transmission in the embedded setting of Fig. 2 is zero: $Y'_{12} = 0$ [31]. Thus, U is also called the unilateral power gain.

In this paper, we are interested in the other property of U which is related to the activity of a device. A device is called active at a certain frequency if it can generate power in the form of single sinusoidal signal at that frequency [27]. It will be shown in the next section that if $U > 1$, the device is active. Similar to other device characteristics, U is also a function of frequency and, in most cases, U decreases with frequency. The frequency that results in $U = 1$ is called the maximum oscillation frequency ($f_{\max}$) [33]. Above this frequency, the device is not active, i.e., it cannot generate any power and hence no oscillation can be sustained. Note that $f_{\max}$ is also the frequency at which maximum available gain (G_{ma}) and maximum stable gain (G_{ms}) become unity [27]. Although G_{ma} and G_{ms} are often used to characterize the frequency response of a device, their shortcoming is that, unlike U, they change with the device embedding.

B. Activity Condition of Two-Port Devices

To find the activity condition, first we find the real power flowing out of a device. For the device in Fig. 1, we can write the total power going into the device as

$$P = V_1^* I_1 + V_2^* I_2 \tag{2}$$

in which "*" denotes the complex conjugate. Using the definition of the admittance matrix

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

we can rewrite (2) as

$$P = Y_{11}|V_1|^2 + Y_{22}|V_2|^2 + Y_{12}V_1^*V_2 + Y_{21}V_1V_2^*. \tag{3}$$

Since we are interested in the sign of P, we can simplify (3) to

$$\frac{P}{|V_1||V_2|} = A^{-1}Y_{11} + AY_{22} + Y_{12}e^{j\phi} + Y_{21}e^{-j\phi} \tag{4}$$

in which

$$A = \frac{|V_2|}{|V_1|}, \quad \phi = \angle \frac{V_2}{V_1}. \tag{5}$$

From (4), the real power (P_R) that flows out of the device can be expressed as

$$\frac{P_R}{|V_1||V_2|} = -(A^{-1}G_{11} + AG_{22}) - |Y_{12} + Y_{21}^*| \cos\left(\angle\left(Y_{12} + Y_{21}^*\right) + \phi\right). \tag{6}$$

For the device to be active, the net power flowing out of the device should be positive, i.e., $P_R > 0$. Therefore, to find the limit of the device activity, we need to find the maximum of the right-hand side of (6). The maximization is in terms of A and ϕ which are the only parameters that are not a function of the device characteristics. There are two cases that we consider for this maximization: If G_{11} or G_{22} is negative, we can maximize the right-hand side of (6) by simply having a very low or

very high A, respectively. This kind of activity is called *negative-conductance activity* and is rarely found in transistors [34]. This is because in most of today's semiconductor processes the stand-alone transistors exhibit positive input and output resistances for a wide range of frequencies. If G_{11} and G_{22} are positive, (6) is maximized by

$$A = A_{\mathrm{opt}} = \sqrt{\frac{G_{11}}{G_{22}}} \tag{7}$$

and

$$\phi = \phi_{\mathrm{opt}} = (2k+1)\pi - \angle\left(Y_{12} + Y_{21}^{*}\right) \tag{8}$$

in which k is an arbitrary integer. By substituting (7) and (8) into (6), we arrive at

$$max\left(\frac{P_R}{|V_1||V_2|}\right) = -2\sqrt{G_{11}G_{22}} + |Y_{12} + Y_{21}^{*}|\,. \tag{9}$$

For the device to be active, (9) should be positive, which means that the activity condition of the device in Fig. 1 can be written as

$$4G_{11}G_{22} < |Y_{12} + Y_{21}^{*}|^{2}\,. \tag{10}$$

This kind of activity is called *transfer activity* and is of particular importance for transistors. Using (1), it can be shown that the condition in (10) is equivalent to [32]

$$U > 1. \tag{11}$$

This is the reason U is used to determine if a device is active at a specific frequency.

As discussed in Section II-A, $f_{\max}$ is the frequency at which U becomes unity. However, based on the above discussion the only way to satisfy the activity condition of (10) and have an oscillator at $f_{\max}$ is for A and ϕ to meet the optimal conditions of (7) and (8). Note that A and ϕ describe the relation between the voltage amplitude and phase of the two ports of the transistor and for a given oscillator topology, they are usually constant. As a result, the maximum frequency of oscillation in a fixed topology can be significantly lower than the device limit. For example in a cross-coupled oscillator the phase difference between gate and drain voltages is set to 180°. If the ϕ_{opt} in (8) is not 180°, then it is impossible to reach an oscillation frequency of $f_{\max}$, even if we use ideal inductors and capacitors.

III. Activity Condition and Oscillator Design

In this section we expand the theory of activity condition to design oscillators with operation frequencies close to the $f_{\max}$ of the active devices. First, we find the maximum frequency of multi-stage ring structures. Note that the popular cross-coupled oscillator is a special case of the ring oscillator with two stages. After that, we present a method to design an oscillator that exploits the full capacity of transistors to achieve the maximum frequency in any given process.

A. Maximum Frequency of Ring Oscillators

Consider an N-stage ring oscillator with inductive loading as shown in Fig. 3. We use inductive loads instead of resistive loads to reduce the power loss and hence increase the maximum frequency of the oscillator [35]. Even though Fig. 3 shows an

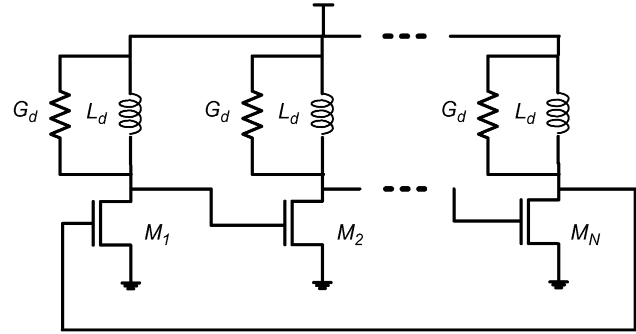


Fig. 3. An N-stage ring oscillator with inductive loading.

oscillator with CMOS transistors, the analysis is valid for any three-terminal device. Fig. 4(a) shows a stand-alone transistor and Fig. 4(b) shows a transistor inside the ring structure. It can be readily seen that the latter has additional conditions on the voltage gain and phase shift compared to the former. Since the goal is to find the maximum oscillation frequency, we can assume that the oscillator operates close to its limit and hence the voltage swing is not large, even at steady-state. This enables us to use small-signal Y parameters. If the voltage swing is not small, as we will discuss in Section III-B, large-signal Y parameters should be used. With this in mind, we can find the voltage gain and phase shift for each section of the ring to be

$$A' = \frac{|V_2'|}{|V_1'|} = 1, \quad \phi' = \angle\frac{V_2'}{V_1'} = k\frac{2\pi}{N} \tag{12}$$

in which k is an integer number. Combining (6), (12), and Y parameters of both networks in Fig. 4, we can write the activity condition of the two-port network in Fig. 4(b) to be

$$\begin{aligned} G_m &= \frac{P_R'}{|V_1'|\,|V_2'|} \\ &= -\left(G_{11} + G_{22} + G_d\right) - |Y_{12} + Y_{21}^{*}| \\ &\quad \times \cos\left(\angle\left(Y_{12} + Y_{21}^{*}\right) + k\frac{2\pi}{N}\right) > 0 \end{aligned} \tag{13}$$

where P_R' is the real power flowing out of the device inside the ring and G_d is the parallel conductance of the inductor. It is interesting that the value of the inductors does not directly appear in (13). The activity condition is only a function of G_d and Y parameters of the stand-alone transistor.

The maximum frequency at which (13) is satisfied is the maximum frequency of oscillation for a ring oscillator with N stages. We call this frequency f_{m-N}. It also results from (13) that at a specific frequency, G_m is the maximum conductance (e.g., maximum G_d) that can be placed across the transistor ports and still sustain the oscillation. If G_d is positive, (13) shows that f_{m-N} is less than the $f_{\max}$ of the transistor. Even if $G_d = 0$, f_{m-N} may be less than $f_{\max}$ because the conditions of (12) may not be the same as the conditions of (7) and (8). As an example, we find f_{m-N} for a cross-coupled oscillator $(N = 2)$ and a three-stage ring oscillator $(N = 3)$ in a 0.13 μm CMOS process:

a) ***Cross-Coupled Oscillator***: For $N = 2$ there are two distinct modes: $k = 0$ and $k = 1$. These correspond to the phase shift of $\phi' = 0°$ and $\phi' = 180°$ per section.

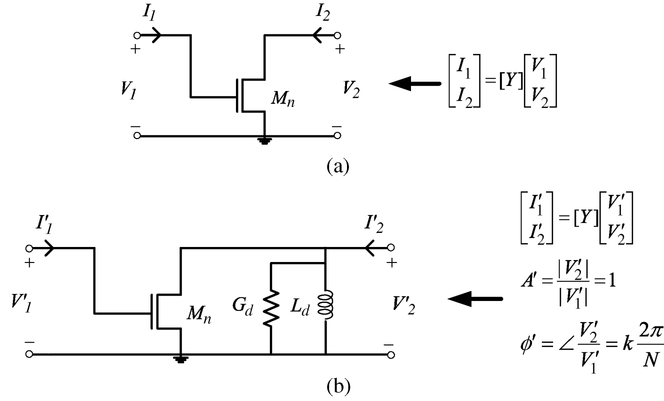


Fig. 4. (a) A stand-alone transistor and (b) a transistor inside a ring oscillator with inductive loading.

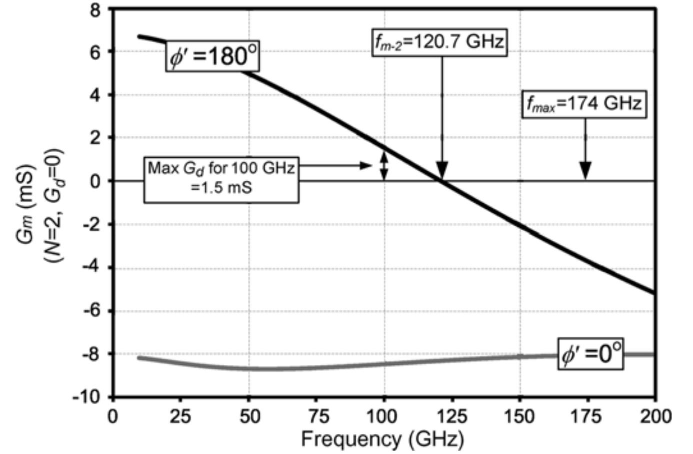


Fig. 5. Simulation of G_m and the maximum frequency of oscillation (f_{m-2}) for a cross-coupled oscillator (two-stage ring oscillator) in the employed 0.13 μm CMOS process.

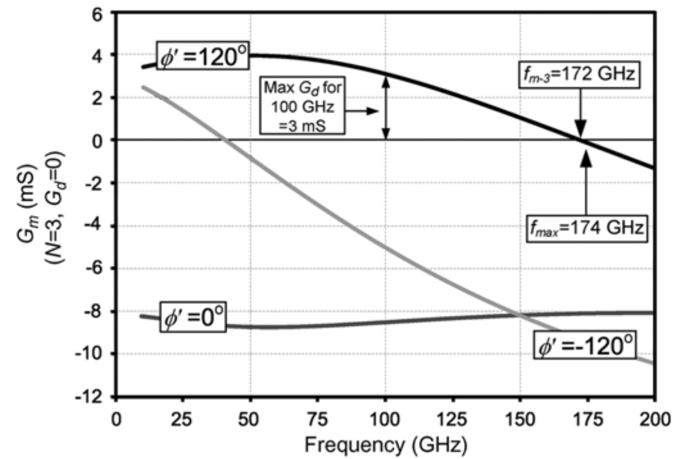


Fig. 6. Simulation of G_m and the maximum frequency of oscillation (f_{m-3}) for a three-stage ring oscillator in the employed 0.13 μm CMOS process.

Here, each oscillation "mode" represents a different phase shift per section that can exist in a ring structure in steady state. Fig. 5 shows the plot of G_m for these two modes using a transistor width of 10 μm with 10 fingers in a common source configuration. The power consumption is 11 mW with power supply and gate-source voltage of $V_{dd} = V_{gs} = 1.5$ V. Fig. 5 shows that no power can flow out of transistor for the mode $\phi' = 0°$ and hence no oscillation would be sustained in that mode. Intuitively this is because in this mode, the current and voltage of the drain are in phase and hence the power that flows into the drain is positive, which means the device is equivalent to a passive component. In the second mode ($\phi' = 180°$) with $G_d = 0$, the oscillator can oscillate through the maximum frequency of oscillation of $f_{m-2} = 120.7$ GHz. The $f_{\max}$ of the transistor is 174 GHz and is much higher than f_{m-2}. This proves that even though $G_d = 0$, maximum frequency of oscillation in a cross-coupled oscillator can not reach the $f_{\max}$ of the transistor in this process. A time domain simulation of a cross-coupled oscillator with $G_d = 0$ verifies the fact that the oscillation frequency cannot exceed 120.7 GHz. In a real circuit, G_d is non-zero and we need to back off from f_{m-2} to have an oscillation. For example Fig. 5 shows that to oscillate at 100 GHz, the inductors can have a maximum G_d of 1.5 mS. As will be discussed in the next section, this will put a limit on the inductor quality factor.

b) ***Three-Stage Ring Oscillator***: Fig. 6 shows G_m for three distinct modes of a three-stage ring oscillator. The same biasing conditions as in Fig. 5 are used in this graph. Here, similar to the cross-coupled oscillator the mode of $\phi' = 0°$ cannot sustain oscillation. The mode $\phi' = -120°$ only results in oscillation for frequencies below 40 GHz. The maximum frequency of oscillation happens for the mode $\phi' = 120°$. f_{m-3} is 172 GHz and is very close to the $f_{\max}$ of the transistors. This is because $\phi' = 120°$ is very close to the condition of (8), which for this process is $\phi' \simeq 112°$. A time domain simulation of a three-stage ring oscillator with $G_d = 0$ verifies that the oscillation frequency can actually reach 172 GHz. As shown in Fig. 6, the maximum G_d for 100 GHz oscillation is 3 mS and is twice the maximum G_d in the cross-coupled oscillator at the same frequency. Furthermore, if both structures oscillate at 100 GHz, the inductors used in the cross-coupled oscillator should be smaller to provide the right phase shift. This leads to higher G_d for the cross-coupled oscillator, given that the inductor quality factors are the same. As it will be discussed in the next section, in this process, the three-stage oscillator will result in a higher voltage swing in almost all frequencies because of the higher G_m as well as lower inductor G_d value for the same frequency.

The same procedure can be applied to any ring oscillator with a phase shift per section of ϕ' to find the maximum frequency of oscillation, f_m. Fig. 7 shows the plot of f_m as a function of ϕ' for the employed CMOS process. Different ϕ' can be achieved by using different number of stages in a ring structure. As examples, the points associated with $N = 2$ and $N = 3$ is annotated in the figure. For other oscillator topologies it is possible to derive voltage amplitude and phase conditions similar to (12) in order to find the maximum frequency of oscillation, f_m. In Section III-C we discuss a methodology to design oscillators that oscillate at frequencies close to the $f_{\max}$ of the transistors.

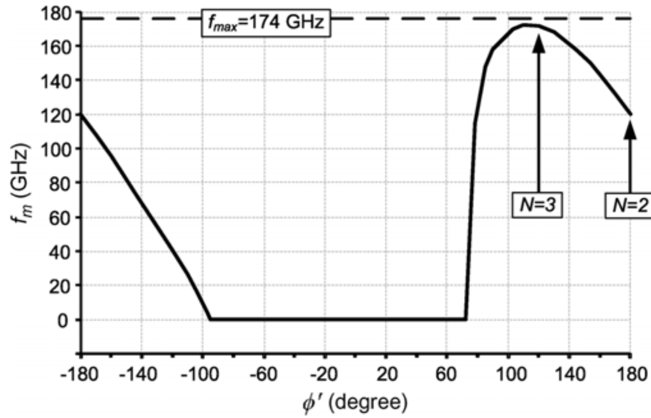
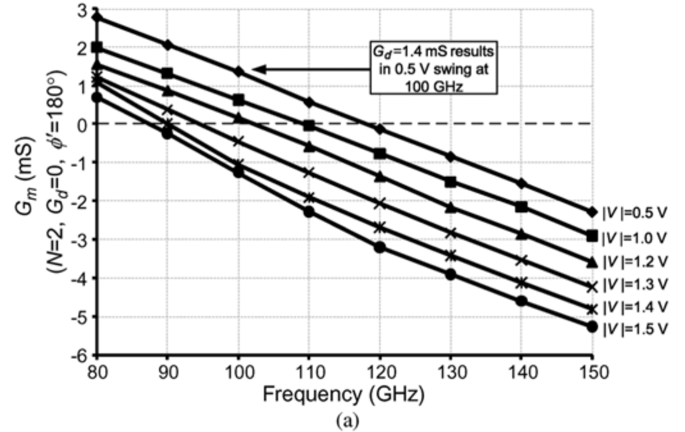


Fig. 7. Simulation of the maximum frequency of oscillation (f_m) of a ring oscillator as a function of phase shift per section (ϕ') in the employed 0.13 μm CMOS process.



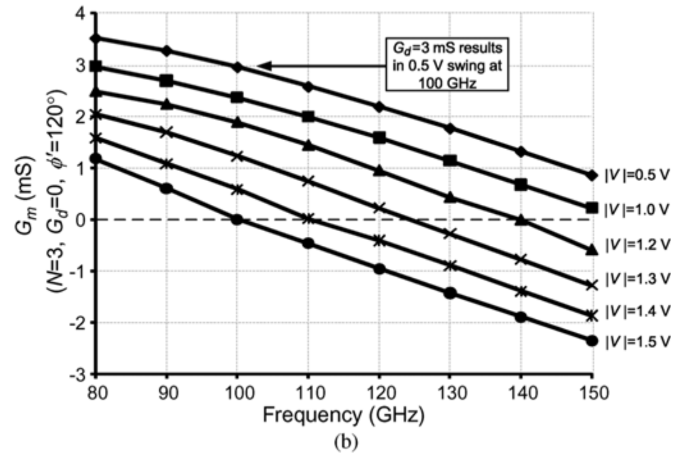


Fig. 8. Simulated large-signal G_m as a function of different voltage amplitudes $(|V| = |V_1'| = |V_2'|)$ in (a) two-stage and (b) three-stage ring oscillators.

B. Voltage Swing of Ring Oscillators

The large-signal dynamics of the ring oscillators can also be explained by using the large-signal Y parameters in the activity condition of (13). P_R' is the real power flowing out of one section of the oscillator and it should be zero at the steady state oscillation. This means that in the steady state, the generated power by the transistor is equal to the power lost in the transistor and the inductor (e.g., G_d). If the small-signal P_R' is positive at a certain frequency, the oscillation is possible at that frequency. This is the start-up condition and it leads to an increase in the voltage swing (e.g., $|V| = |V_1'| = |V_2'|$) of the section in Fig. 4(b). As the voltage amplitude increases, the Y parameters of the transistor also changes to the extent that P_R' or G_m in (13) becomes zero. At this point the voltage amplitude stays constant and an steady state oscillation is reached. As an example, Fig. 8 shows the simulated large-signal G_m for two- and three-stage ring oscillators in the same 0.13 μm CMOS process. The Y parameters of the section in Fig. 4(b) is simulated for different voltage amplitudes, $|V| = |V_1'| = |V_2'|$, and are inserted in (13) to find G_m of Fig. 8. As the voltage amplitude increases, the G_m curve starts to move down until it crosses the zero line at the oscillation frequency. For example if both two- and three-stage oscillators are set to oscillate at 100 GHz using ideal inductors, Fig. 8 shows that the two- and three-stage oscillators will have a voltage swing of around 1.2 V and 1.5 V, respectively. A time domain oscillator simulation verifies the exact predicted voltage swings for both oscillators.

Repeating the same example for different frequencies shows that the three-stage oscillator results in higher voltage swing than the two-stage structure. This is because the starting small-signal G_m value is lower for the two-stage ring (as we saw in Section III-A) and the G_m curve variation for different voltage amplitudes are almost the same for both oscillators. Since G_d is a linear conductance associated with the inductor, it can be linearly subtracted from the curves in Fig. 8 to find the voltage swings. For example in the two- and three-stage rings, a voltage swing of 0.5 V can be achieved at 100 GHz if the G_d of 1.4 mS and 3 mS is used, respectively.

C. Design Methodology of High-Frequency Fundamental Oscillators

Higher order harmonic oscillators with frequencies close to and beyond the $f_{\max}$ of the transistors have been reported [20], [36], [37]. However, most of these designs use push-push structures to utilize the second harmonic of the fundamental oscillation frequency. This results in low output power and hence fundamental oscillators are more desirable for high power generation. Using the theory discussed in the previous sections, we introduce a method to take full advantage of the transistor capabilities to design high-frequency fundamental oscillators. Here is the design methodology:

1) *Find the $f_{\max}$ of the process*: This can be done by measurement or simulation. In the case of simulation, it is noteworthy that because $f_{\max}$ is often obtained from extrapolation, it is usually higher than the actual value [22]. Also, $f_{\max}$ is layout dependent, so the same layout that was used in finding $f_{\max}$ should be used in the rest of the design process. Finally, to maximize $f_{\max}$, we need to use multiple fingers and avoid a large transistor width [22].
2) *Choose an oscillation frequency $(f_{\rm osc})$ below $f_{\max}$*: That is if an oscillation frequency is desired. If the objective is to maximize the frequency, we pick an initial value and if, in the next steps, we find that the passive components are good enough, we come back to increase the frequency.

3) *Find A_{opt} and ϕ_{opt} at f_{osc} using* (7) *and* (8): If these conditions are met, the maximum conductance (G_d) can be placed at the transistor ports at f_{osc}. Since simulation shows that (7) and (8) are not strong functions of the transistor width, the same transistor used in step 1 can be used here.
4) *Find an oscillator topology that satisfies the A_{opt} and ϕ_{opt} values*: These values can be satisfied by the inherent characteristics of the topology, e.g., in a ring oscillator, or by tuning the passive components of the oscillator, e.g., in Colpitts oscillator. Sometimes it is hard to achieve the exact values of A_{opt} and ϕ_{opt}, but it still boosts the frequency if A and ϕ are close to the optimum values.
5) *Choose the transistor width and passive component values*: This part can be done using ideal passive components. Based on the chosen topology, f_{osc}, and the power budget, we can find the component values and sizes. Usually another restriction exists for the sizes of the transistor and passive components. If the transistor is too large, the corresponding inductor/capacitor size becomes too small and comparable with the parasitics, making it hard to design and control, specially at high f_{osc}. After choosing the transistor size we need to find its f_{max} and make sure it is still higher than f_{osc}. If not, we need to go back to step 2 and reduce the f_{osc}.
6) *Find the maximum conductances that can be placed at the transistor ports at f_{osc}*: Having the topology and the component values, we can find the actual A and ϕ that can be slightly different than A_{opt} and ϕ_{opt}. For example, in ring oscillators the maximum conductance, G_d, can be found using $A = 1$, $\phi = k2\pi/N$, and (13). We can model most of the other oscillators as an active device embedded in a passive network, as shown in Fig. 9. Here G_{11}^p and G_{22}^p represent the loss of termination at the input and output of the transistor. The maximum conductances that can sustain the oscillation are the maximum G_{11}^p and G_{22}^p and their ranges can be found using

$$\left(A^{-1}\left(G_{11}+G_{11}^{p}\right)+A\left(G_{22}+G_{22}^{p}\right)\right)+\left|Y_{12}+Y_{21}^{*}\right| \times\cos\left(\angle\left(Y_{12}+Y_{21}^{*}\right)+\phi\right)<0 \quad (14)$$

which was derived from (6).
7) *Design the passive components to satisfy* (14): In this step, we replace the ideal passive components with real ones. Since we know their values from step 5, we only need to maximize their quality factor, e.g., by using E/M techniques. If the conductance value that models the loss of passive components (such as G_d or G_{11}^p and G_{22}^p) is larger than the maximum allowed conductance in step 6, it means that the oscillation is not possible. In this case, we need to go back to step 5 and increase the size of the transistors and repeat steps 6 and 7. But if we are already at the maximum size of the transistors based on the restrictions in step 5, then we conclude that the oscillation in the selected f_{osc} is not possible in this process and we need to go back to step 2 to lower f_{osc}. On the other hand, if G_{11}^p and G_{22}^p satisfy (14), then the oscillation is possible. We can simulate the oscillator and verify that the voltage swing is large enough. If not, we need to go back to step 5 or 2 to increase the transistor size or reduce the oscillation frequency. Finally, if the voltage swing is more than is required, we can go back to step 5 and reduce the transistor size to lower the power consumption for the same frequency or go back to step 2 and increase the oscillation frequency.

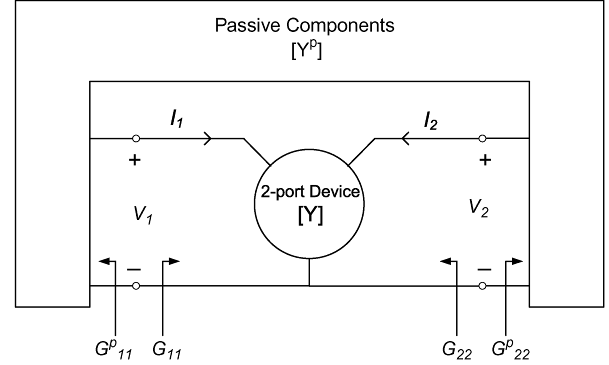


Fig. 9. Active device embedded in a passive network.

The flowchart of the above methodology is illustrated in Fig. 10. It is also noteworthy to mention that if there are any phase noise considerations, one can always choose a topology in step 4 or choose a transistor size in step 5 to trade off the oscillation frequency or power consumption with a better phase noise performance.

IV. 121 GHz and 104 GHz Fundamental Oscillators

A. Design and Simulation

Using the above methodology we design two fundamental oscillators at 120 GHz and 105 GHz in a 0.13 μm CMOS process. Starting from step 1, we find the f_{max} of the process to be 174 GHz. This number is simulated for a 10 μm wide transistor with 10 fingers and the biasing condition of $V_{ds} = V_{gs} = 1.5$ V. As mentioned before, this f_{max} is based on extrapolation and is more than the typical measured value, which is around 135 GHz [28]. We choose 120 GHz and 105 GHz as oscillation frequencies because they are higher than any reported fundamental oscillation frequency in a 0.13 μm CMOS process and are also lower than the typical f_{max}. For step 3 we plot A_{opt} and ϕ_{opt} as a function of frequency in Fig. 11. For both frequencies, A_{opt} and ϕ_{opt} are around 1 and 120°, respectively. Therefore, the simplest and closest topology for step 4 is a three-stage ring oscillator. Next, in step 5 we use the topology of Fig. 12 to size the transistors and inductors. For initial sizing, the buffer is disconnected from the oscillator. Based on the power budget and reasonable inductor size, we choose $W_1 = 10$ μm with 10 fingers for each transistor, which corresponds to a power consumption of 22 mW for the oscillator. The transistor is implemented using a conventional double gate connection and a substrate contact ring around the transistor as shown in Fig. 13(a). Using the transistor size, the inductors would be $L_d = 70$ pH and $L_d = 90$ pH for an f_{osc} of 120 GHz and 105 GHz, respectively. In step 6 we need to go back to Fig. 6 and find G_m which is the maximum G_d that can sustain the oscillation. This figure is plotted for $A = 1$, $\phi = 120°$, and the same transistor size. G_m is 2.4 mS and 2.9 mS for f_{osc} of 120 GHz and 105 GHz,

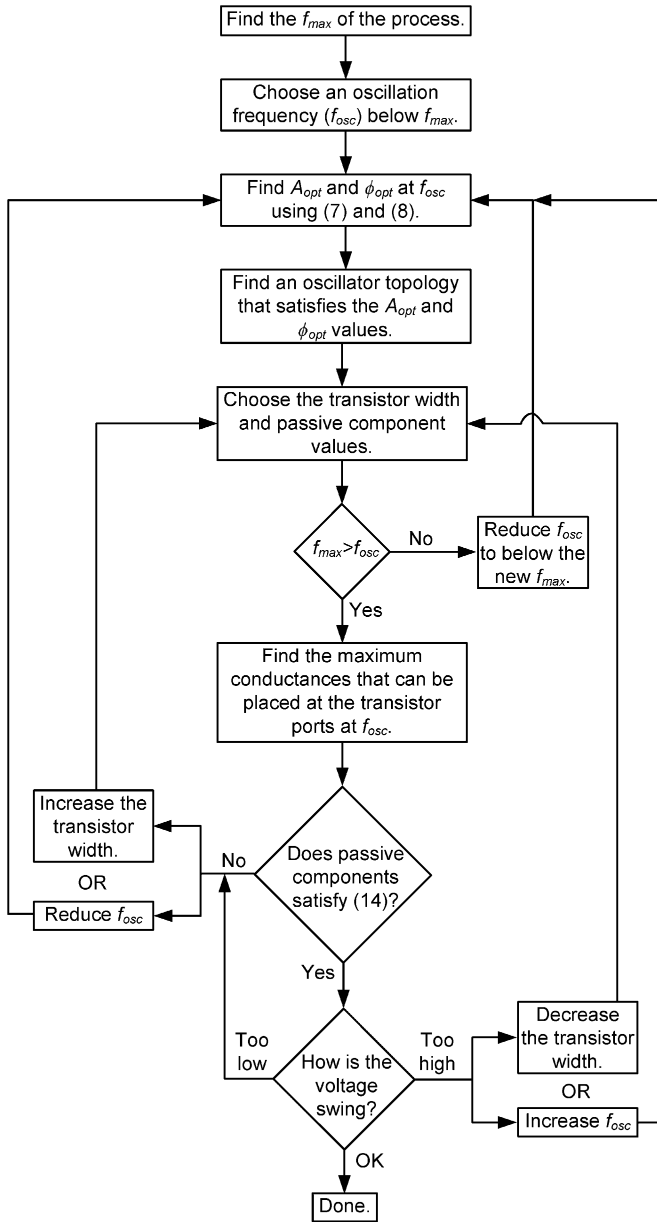


Fig. 10. Flowchart of the proposed design methodology for high-frequency fundamental oscillators.

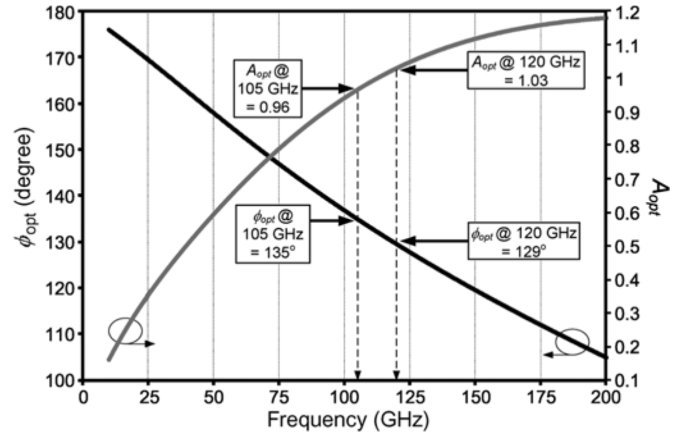


Fig. 11. Simulation of the optimum A and ϕ for a 0.13 μm CMOS transistor.

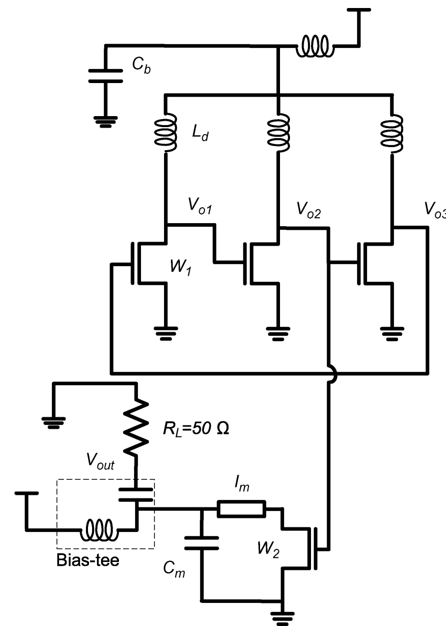


Fig. 12. A three-stage ring oscillator with buffer.

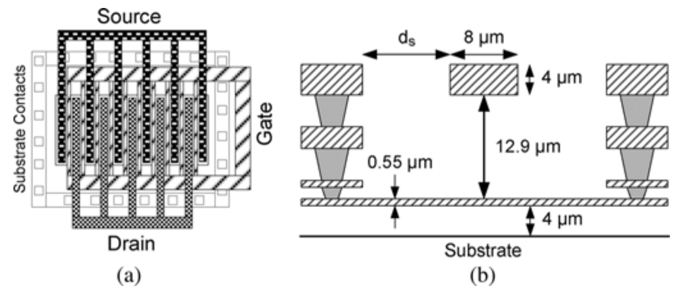


Fig. 13. (a) Layout of a double-gate connection transistor that is used in all the oscillators and (b) cross section of the shielded coplanar transmission line in the employed 0.13 μm CMOS process.

respectively. Having the maximum G_d and the inductor sizes from step 5, we can find the minimum allowed quality factor of the inductors to be 8 and 6 for $L_d = 70$ pH and $L_d = 90$ pH, respectively. Using Sonnet electromagnetic simulator, we design high quality factor inductors in step 7. To do so, we use shielded coplanar transmission lines as inductors and achieve quality factors of 30 and 26 for $L_d = 70$ pH and $L_d = 90$ pH, respectively. These values are higher than the minimum required quality factors (8 and 6) and therefore oscillation is possible. The cross section of the shielded coplanar transmission lines is presented in Fig. 13(b). In this Figure d_s is the distance between the shield and the signal line and varies between 6 μm to 13 μm for different inductor values.

At this point we can go back to step 2 and increase the oscillation frequency. However, we decide to keep the frequencies at 120 GHz and 105 GHz because as additional loss is added to the circuit from vias and connections, the quality factor of the inductors drops. Furthermore, we require a high voltage swing in order to deliver high output power. As shown in Fig. 12, a small buffer transistor size of $W_2 = 2$ μm is used to minimize the loading of the oscillator. The buffer consumes 2.7 mW from

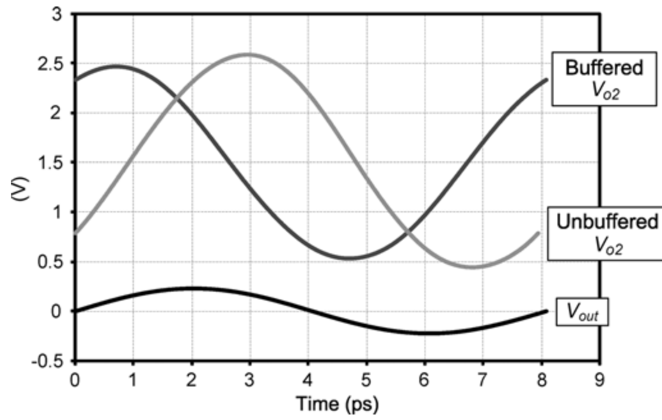


Fig. 14. Simulation of one period of $V_{\rm out}$, buffered V_{o2} and unbuffered V_{o2} signals in time domain for the 123 GHz oscillator.

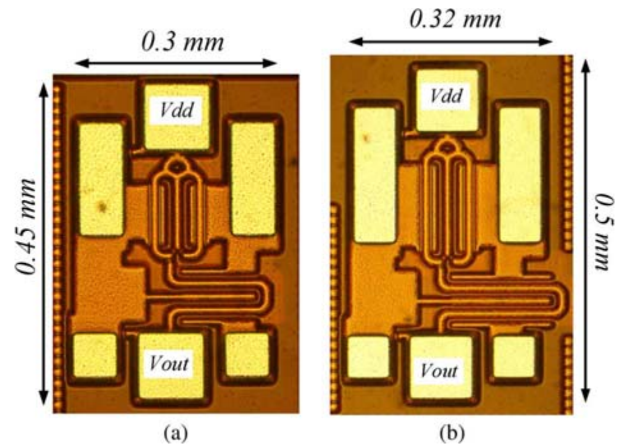


Fig. 15. Die photo of the fundamental oscillators at (a) 121 GHz and (b) 104 GHz.

a 1.5 V supply. To match the buffer to the 50 Ω load, a transmission line similar to that of Fig. 13(b) with $d_s = 10$ μm and length of l_m along with a capacitor, $C_m = 62$ fF, are used. The matching capacitor, C_m, and the DC supply bypass capacitor, C_b, were constructed using the metal-to-metal capacitors of the probing pads and hence a quality factor of 150 is achieved at 120 GHz. The length of matching transmission lines are $l_m = 340$ μm and $l_m = 415$ μm for the 120 GHz and 105 GHz oscillators and they both have the electrical length of around $\lambda/2$. For these oscillators, the first and second harmonics are out of phase and will be canceled out at the V_{dd} line [29]. However, the third harmonic exists at the V_{dd} line and will be suppressed by C_b.

All of the lines and pads are simulated using Sonnet, and Cadence Spectre was used to find the output frequency and power. After a careful simulation, the output power of −3 dBm and −2 dBm were achieved at 123 GHz and 107 GHz. Fig. 14 shows the simulation of one period of $V_{\rm out}$, buffered V_{o2} and unbuffered V_{o2} signals in time domain for the 123 GHz oscillator. Because of the small buffer transistor, the V_{o2} amplitude and frequency do not change very much with the buffer. For the same reason the voltage gain of the buffer is only 0.25. Simulation shows that adding the buffer introduces a maximum phase change of 4° between the output nodes (V_{o1}, V_{o2} and V_{o3}). Phase noise of −85 dBc/Hz and −90 dBc/Hz at 1 MHz offset was simulated for 123 GHz and 107 GHz oscillators, respectively. The power of all other harmonics are at least 45 dB lower than the fundamental signal in both oscillators.

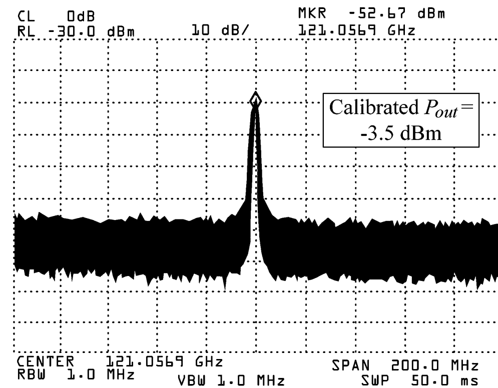


Fig. 16. The measured IF spectrum of the 121 GHz oscillator.

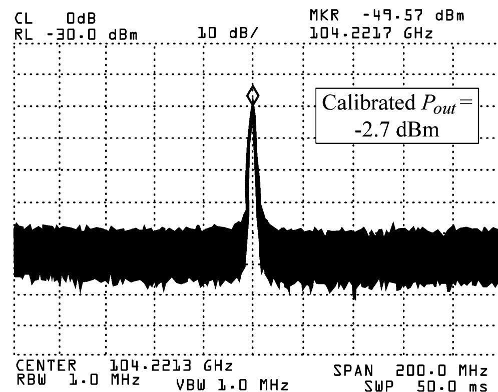


Fig. 17. The measured IF spectrum of the 104 GHz oscillator.

B. Measurement Results

The fundamental oscillators were fabricated in a 0.13 μm CMOS technology. Fig. 15 shows the chip photo of these oscillators. A WR-08 GSG Picoprobe with a built-in bias-tee was used to probe the output of these oscillators. Based on the factory data, the insertion loss of the probe is around 2 dB at the measured frequencies. Next, we mix down the signal using an OML WR-08 harmonic mixer and connect the IF port of the mixer to the Agilent 8564EC spectrum analyzer. The oscillation frequency was found by sweeping the LO frequency and measuring the IF frequency change [21]. The measured oscillation frequency for the two oscillators are 121 GHz and 104 GHz, which are in good agreement with the simulation results. Based on the factory data sheet, the typical conversion loss of the harmonic mixer is 47.2 dB and 45 dB at 121 GHz and 104 GHz, respectively. Figs. 16 and 17 show the measured output spectrum of the two oscillators. Based on the loss of the measurement setup, the peak output powers are −3.5 dBm and −2.7 dBm at 121 GHz and 104 GHz, respectively. The measured results are close to the simulation presented in the previous section. The DC power consumption including the output buffer is 21 mW from a 1.28 V supply and 28 mW from a 1.48 V supply for 121 GHz and 104 GHz oscillators, respectively. The phase noise

at 1 MHz offset frequency was measured to be −88 dBc/Hz and −93.3 dBc/Hz for the 121 GHz and 104 GHz oscillators, respectively. Table I shows a comparison of this work with the state of the art. To the best of the authors' knowledge, the 121 GHz and the 104 GHz oscillators have the highest output power in any CMOS oscillator and the 121 GHz oscillator has the highest frequency among 0.13 μm CMOS fundamental oscillators.

V. 256 GHz AND 482 GHz TRIPLE-PUSH OSCILLATORS

For many terahertz applications the target frequency is larger than the maximum oscillation frequency and hence it is desirable to make oscillators beyond the $f_{\max}$ of transistors. One example is using conventional CMOS process in the terahertz band. To do so, we need to use higher order harmonic oscillators rather than fundamental oscillators. Push-push oscillator is the most common topology for oscillation beyond $f_{\max}$ [20], [25]. It collects the second harmonic of the fundamental component and is usually implemented using a cross-coupled oscillator. Recently CMOS harmonic oscillators including push-push structures have been reported at around 300 GHz and beyond [17], [19], [20]. However the reported output power is less than −45 dBm which is low for most practical applications. Low output power of CMOS terahertz oscillators is one of the major reasons of why CMOS has not been used to implement a complete terahertz transceiver. In this section, we use two major techniques to boost the power and achieve −17 dBm at 256 GHz and −7.9 dBm at 482 GHz in CMOS: 1) We use the theory introduced above to generate higher power and voltage swing at fundamental frequency and 2) efficiently transfer the power of the third harmonic from the transistors to the load.

A. A Triple-Push Oscillator in 0.13 μm CMOS

As discussed in Section III, in the employed 0.13 μm CMOS process, a three-stage ring oscillator can reach a higher oscillation frequency and at the same time provide a higher voltage swing compared to a cross-coupled oscillator. Higher voltage swings at the transistor ports increase its nonlinearity. Therefore, a harmonic oscillator that is based on a three-stage ring structure leads to higher frequency and power than the push-push oscillator. Furthermore, since the three-stage ring oscillator has one more transistor than the push-push oscillator, it can potentially generate even more output power. The other advantage of the three-stage ring over a push-push structure is that because the phase shift per section is 120°, the same fundamental frequency requires larger inductors, making them easier to characterize and implement. The proposed topology is shown in Fig. 18. In this circuit, the phase shift per section is 120° and therefore the third harmonic of the fundamental frequency from all three transistors is in phase and hence it adds up constructively at the output node, V_{out}. For the same reason, all the harmonics that are not multiples of 3 (e.g., first, second, fourth, etc.) are out of phase and cancel out at node V_{out}. This kind of harmonic oscillator that adds up the third harmonic of the fundamental oscillation at the output is called triple-push [29], [30].

Although the topology in Fig. 18 can achieve high frequencies in fundamental oscillation, it is not optimized for high power harmonic generation. To increase the voltage swing

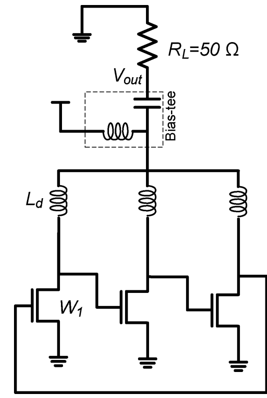


Fig. 18. A triple-push oscillator based on a three-stage ring.

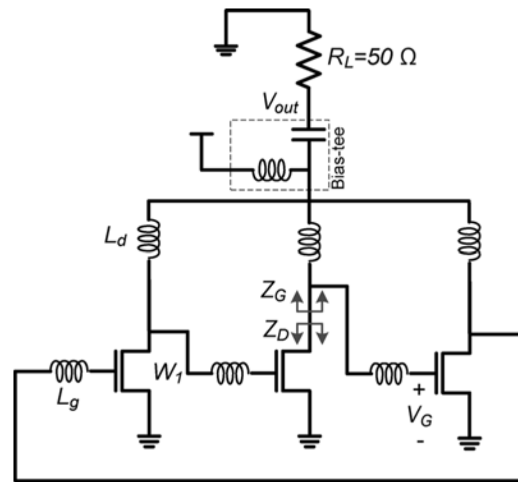


Fig. 19. Enhanced triple-push oscillator for high power generation.

and hence generate a stronger third harmonic, we propose the topology of Fig. 19. Let us assume a fundamental oscillation frequency of 85 GHz which results in the output frequency of 255 GHz. From Fig. 11 we know that the optimum conditions for a stand-alone transistor at 85 GHz are $A_{\text{opt}} = 0.84$ and $\phi_{\text{opt}} = 144°$. However, in a regular three-stage ring in Fig. 18 $A = 1$ and $\phi = 120°$. By using an inductor in the gate of the transistor as in Fig. 19 we can get closer to the optimum values: The inductor delays the voltage and can change ϕ from 120° to the optimum value of 144°. The inductor also resonates with the input capacitance of the transistor and increases the gate voltage to reduce A (i.e., voltage gain of a stand-alone transistor) from 1 to the optimum value of 0.84.

To find the optimum L_g we redraw a transistor and its gate inductor in Fig. 20. Because the two-port network in Fig. 20 is a section of the oscillator shown in Fig. 19, the gain and phase shift of this stage are $A' = 1$ and $\phi' = 120°$. Therefore, the activity condition of the network in Fig. 20 can be found from (6) to be

$$\begin{aligned} G_m &= \frac{P'_R}{|V'_1|\,|V'_2|} \\ &= -\left(G'_{11} + G'_{22}\right) - |Y'_{12} + Y'^{*}_{21}| \\ &\quad \times \cos\left(\angle\left(Y'_{12} + Y'^{*}_{21}\right) + 120°\right) > 0 \end{aligned} \tag{15}$$

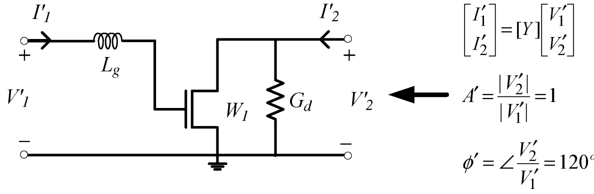


Fig. 20. The model of one section of the enhanced triple-push oscillator used to optimize the gate inductor value.

where Y'_{ij}'s are the elements of the admittance matrix of the network, $G'_{ij} = \mathrm{Real}[Y'_{ij}]$, and $i, j = 1, 2$. As discussed in Section III-A, G_m is not a direct function of L_d and that is why it is not included in Fig. 20. G_m in (15) is plotted in Fig. 21 for different gate inductor values and $G_d = 0$. To take into account the effect of inductor loss, we construct L_g using a shielded coplanar transmission line with $d_s = 5\ \mu$m and a resulting quality factor of around 30 at 85 GHz. In this plot, the width of the transistor is $W_1 = 20\ \mu$m with 20 fingers. Fig. 21 shows that at lower frequencies, the G_m increases with L_g. For example, at 85 GHz, G_m goes from 7 mS to 15 mS as L_g goes from zero to 55 pH. This also implies that for a fixed loss, i.e., fixed G_d, and fixed $|V'_1|$ and $|V'_2|$ at 85 GHz, the transistor shown in Fig. 20 generates more power for a higher L_g. This higher power generates higher gate voltage swing that results in stronger harmonic generation. For a fair comparison, it should be mentioned that for $L_g = 0$ and $L_g = 55$ pH, the required L_d to keep the oscillation frequency at 85 GHz is $L_d = 68$ pH and $L_d = 45$ pH, respectively. Thus, for a fixed oscillation frequency, as L_g increases, L_d decreases and its corresponding loss, i.e., G_d, increases if the quality factor of different L_d's is the same. In our example, for $L_d = 68$ pH and $L_d = 45$ pH fortunately the increase in $G_d = L_d\omega/Q$ (68 pH$/45$ pH $\simeq 1.5$) is less than the increase in G_m (15 mS$/7$ mS $\simeq 2.1$ from Fig. 21) and hence the voltage swing is higher with $L_g = 55$ pH compared to $L_g = 0$. Optimum L_g of 55 pH results in maximum G_m in Fig. 20. Similarly, maximum gate voltage swing in the oscillator in Fig. 19 happens for around the same L_g value. The gate voltage amplitude at 85 GHz changes from 1.1 V with no L_g to 1.8 V with $L_g = 55$ pH in Fig. 19. Note that a gate inductor that tunes out the gate capacitor at 85 GHz and results in the highest voltage swing at the gate in the open loop structure is around 120 pH. However, based on Fig. 21, L_g of greater than 85 pH results in a very low or even negative G_m at 85 GHz and therefore the transistor can not support the high voltage swing for $L_g = 120$ pH. This means that for each frequency there is a minimum L_g value that results in a negative G_m and makes the oscillation impossible as shown in Fig. 21. In the actual design, the gate inductor should be adequately smaller than this value. To summarize, as shown in Fig. 21, there is a trade-off between the maximum frequency of oscillation and the power at lower frequency as we change the value of L_g.

The gate inductor L_g also helps extract the harmonic power from the transistor. As shown in Fig. 19, Z_D is the impedance looking into the drain of the transistor and Z_G is the impedance looking from the drain of the transistor. If Z_D and Z_G are matched at the third harmonic then the transistor delivers the maximum power at this frequency. Assuming that the loss at the gate of the transistor is much lower than the loss at the load, R_L, then after matching Z_D and Z_G, most of the power from the device flows to the load. Fig. 22 shows the reflection coefficient at the drain of the transistor with and without an optimum L_g for matching the third harmonic. Here, the definition of the reflection coefficient for complex impedances is used [38]. Using an optimum L_g of 20 pH we can achieve the minimum drain reflection coefficient of -9 dB at 255 GHz while the fundamental oscillation frequency is kept at 85 GHz. Without using any L_g the reflection coefficient is -2.2 dB at 255 GHz.

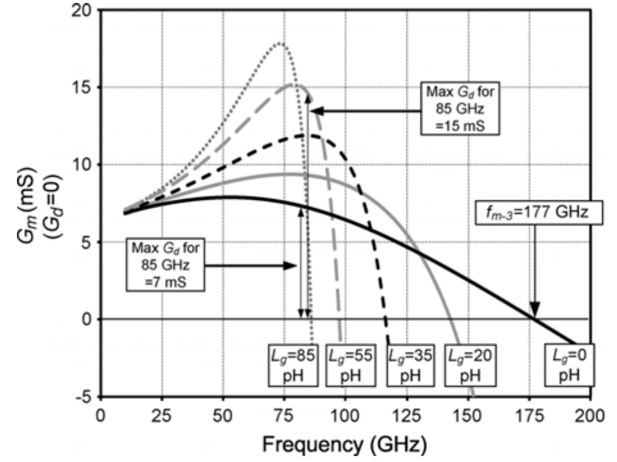


Fig. 21. Simulation of G_m of one section of the enhanced triple-push oscillator shown in Fig. 20 with different L_g values using the 0.13 μm CMOS process.

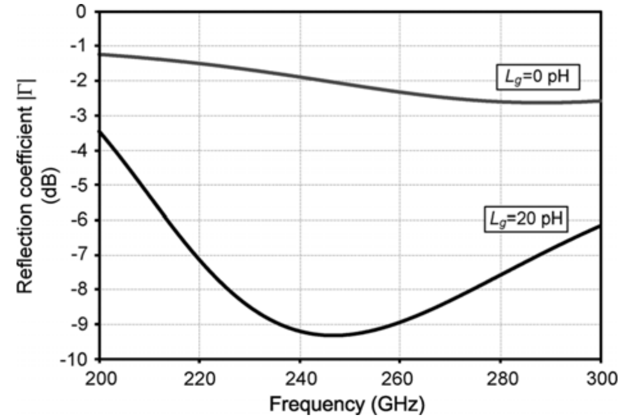


Fig. 22. Simulated reflection coefficient at the drain of the transistor with and without the gate inductor, L_g.

In the designed prototype we select $W_1 = 20\ \mu$m to increase the third harmonic power and have a reasonable inductor size. L_g and L_d are constructed using shielded coplanar and microstrip transmission lines, respectively. As discussed, L_g can improve both harmonic generation and matching at the same time. However the optimum L_g values for harmonic generation and matching are different. Initial simulation shows that with the optimum component values of $L_g = 30$ pH and $L_d = 50$ pH, the circuit generates maximum power of -3 dBm at 255 GHz. Fig. 23 shows the gate voltage (V_G) and output voltage (V_{out}) in time domain for $L_g = 0$ and the optimum case of $L_g = 30$ pH. By using this value of L_g, the output power increases by 6 dB.

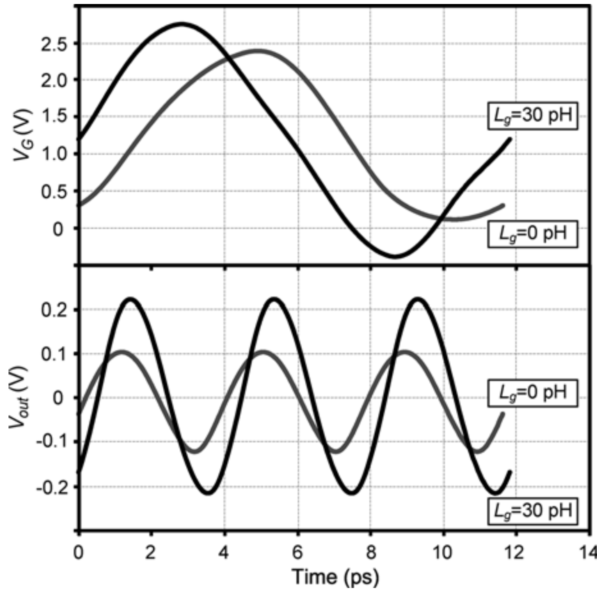


Fig. 23. Simulated gate voltage (V_G) and output voltage (V_{out}) in time domain for $L_g = 0$ and the optimum case of $L_g = 30$ pH.

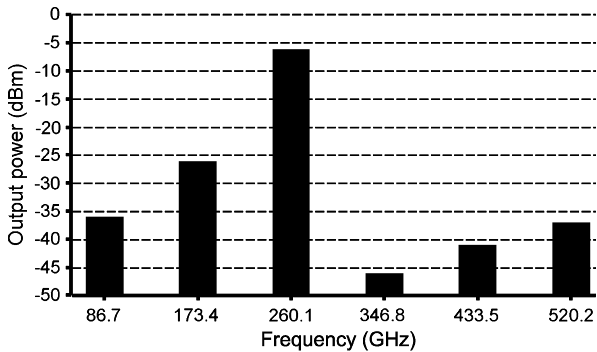


Fig. 24. Simulated output spectrum for the 260 GHz oscillator in the 0.13 μm CMOS process.

In order to maintain the symmetry of the layout, we had to deviate from the optimum inductor values. All of the lines, connections, and pads were simulated in the Sonnet electromagnetic simulator. The final simulation shows that the oscillator frequency has a small shift to 260 GHz with -6.4 dBm of power with a DC power consumption of 36 mW from a 1.2 V power supply. The phase noise is simulated to be -83 dBc/Hz at 1 MHz offset. The output spectrum is shown in Fig. 24. All of the harmonics are at least 20 dB below the 260 GHz component. Fig. 24 is based on the actual layout simulation that includes all of the non-symmetric effects of parasitics and lines.

B. A Triple-Push Oscillator in 65 nm CMOS

Using the same approach, we design and simulate a triple-push 450 GHz oscillator in a 65 nm CMOS process. The fundamental frequency is around 150 GHz. Fig. 25 shows the simulated optimum A and ϕ (A_{opt} and ϕ_{opt}) as a function of frequency for a transistor with bias current of 12.5 mA and width of W $= 20$ μm with 20 fingers in a 65 nm CMOS process. The

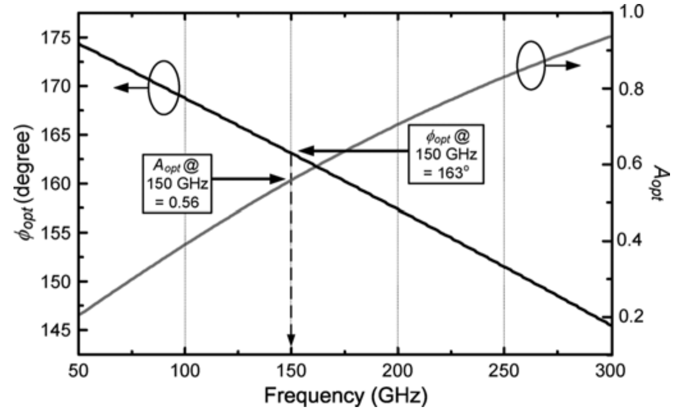


Fig. 25. Simulation of the optimum A and ϕ of a stand-alone transistor in a 65 nm CMOS process.

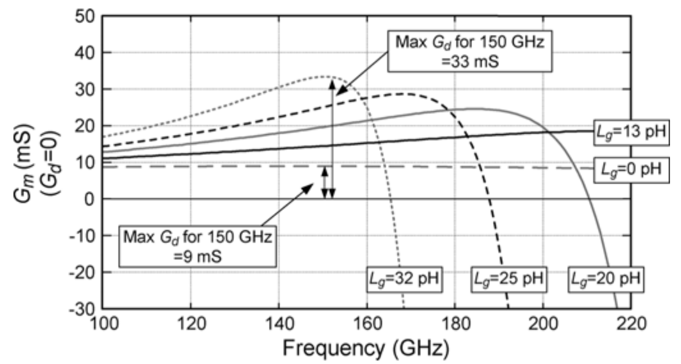


Fig. 26. Simulation of G_m of one section of the enhanced triple-push oscillator shown in Fig. 20 with different L_g values using the 65 nm CMOS process.

transistor is implemented using a conventional double gate connection and a substrate contact ring around the transistor similar to Fig. 13(a). The optimum values at 150 GHz are $A_{\mathrm{opt}} = 0.56$ and $\phi_{\mathrm{opt}} = 163°$. As discussed in the previous section, by adding an inductor in the gate of the transistor we can get closer to these optimum values. The activity condition of a two-port network similar to that of Fig. 20 is plotted in Fig. 26. G_m is plotted for different L_g values which are realized using microstrip transmission lines with a signal metal thickness of 1.3 μm and distance between the signal metal layer and the ground layer of 5.9 μm. The quality factor of the inductors are around 20 at 150 GHz. It is shown in Fig. 26 that the G_m changes from 9 mS to the maximum value of 33 mS at 150 GHz by adding a gate inductor of $L_g = 32$ pH. As discussed, this gate inductance also results in a maximum voltage swing at the gate of the transistors.

For optimum matching at the third harmonic, the L_g should be around 13 pH. This value results in drain reflection coefficient of -18 dB at 450 GHz. Without L_g, the reflection coefficient increases to -1 dB at 450 GHz. In both cases the output frequency is kept constant at 450 GHz by changing the drain inductor, L_d, which is realized by using the same microstrip transmission line as L_g. The final design employs transistor size of 20 μm and inductor values of $L_g = 17$ pH and $L_d = 26$ pH to reach an optimum voltage swing and power matching for maximum output power. Simulation shows -3 dBm of power at 450 GHz while

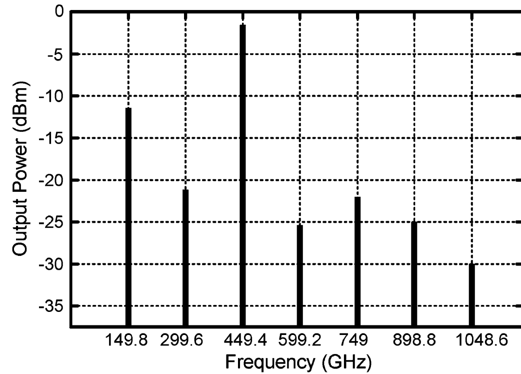


Fig. 27. Simulated output spectrum of the 450 GHz oscillator in the 65 nm CMOS process.

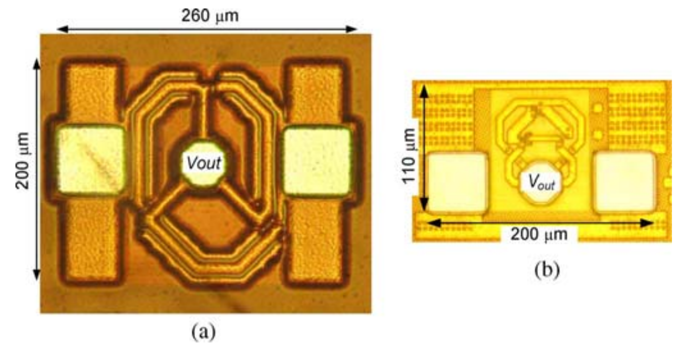


Fig. 28. Chip photo of the (a) 256 GHz and (b) 482 GHz oscillators.

consuming 38 mW of DC power from a 1.2 V supply. The simulated output spectrum is shown in Fig. 27. Without using L_g, the simulated power is 18 dB lower at the same frequency.

C. Measurement Results

Fig. 28 shows the die photos of the triple-push oscillators. Fig. 29(a) shows the test setup for the frequency measurement of the 482 GHz oscillator. A Cascade i500-GSG probe with a built in bias-tee is used to probe the output signal as shown in Fig. 29(a). If we had an on-chip antenna to extract the power from the oscillator we could eliminate the bypass capacitor of the bias-tee since on-chip antennas usually have a series capacitor and block any DC current. Simulation shows that if we use a 50 Ω on-chip antenna, the RF choke of the bias-tee can be replaced by a 150 μm on-chip microstrip transmission line. This adds only around 0.1 dB of loss to the output signal. Therefore, we can replace the probe with an on-chip antenna and have a similar performance in both triple-push oscillators. As shown in Fig. 29(a) a VDI WR-2.2EHM harmonic mixer is connected to the probe to mix down the signal. By sweeping the LO frequency and observing the IF, the LO harmonic number and the signal frequency can be determined. The output frequency was measured to be 482.1 GHz. The difference between simulation and measurement is due to inaccuracy in device models as well as overestimation of the effect of vias. The IF spectrum of the signal is shown in Fig. 30(a) when the 16th harmonic of the LO frequency is used. In this figure, the power consumption is 35 mW from a 1.2 V supply. The phase noise is measured to be -76 dBc/Hz at 1 MHz offset as shown in Fig. 30(b). Using the same setup we are able to observe the second harmonic at 321.4 GHz that is very close to the lower cut-off frequency of the WR2.2 waveguide. The loss of the probe and all the other components are calibrated using network analyzer by Cascade and VDI. The loss of the probe is 9 dB at 482 GHz and 7 dB at 321 GHz, and the conversion loss of the mixer is 44 dB and 35 dB for the 16th harmonic of the LO when the signal is at around 482 GHz and 321 GHz, respectively. Using these values, we found the power of the third harmonic to be 15.5 dB higher than the second harmonic. With the same setup as Fig. 29(a), we measured the output power at 482 GHz versus DC power shown in Fig. 31. To be more accurate, we also used an Erickson PM4 power meter as illustrated in Fig. 29(b). This measured output power is also shown in Fig. 31. The measured output power with 35 mW DC power consumption from a 1.2 V supply is -8.6 dBm which is 5.6 dB lower than the simulated output power with similar DC power. This is mainly because of the inaccurate device models at this frequency range. When the DC power consumption increases to 61 mW the peak output power of -7.9 dBm at 482 GHz is achieved. To the best of the authors' knowledge, the output power is the highest among CMOS and SiGe sources and is comparable with oscillators using InP HEMT and InP HBT. Table I shows the comparison of this work with the state of the art.

A similar test setup as in Fig. 29 was used to measure the output frequency and power of the triple-push oscillator in 0.13 μm CMOS. A Cascade Infinity WR-03 GSG probe with 5 dB loss at around 260 GHz was used to measure the output. The probe has a built-in bias-tee, which was used to bias the circuit from the output node. The signal is mixed down using an OML WR-03 harmonic mixer. To measure the output frequency, we used the same method described for the 482 GHz oscillator. Based on this method, the output frequency is measured to be 256 GHz. Fig. 32 shows the IF spectrum of this oscillator when the 48th harmonic of the LO frequency is used and the DC power consumption is 38 mW from a 1.25 V supply. Because of the high conversion loss of the harmonic mixer, the power received by the spectrum analyzer is low and hence it is hard to measure the phase noise directly from the 256 GHz signal. Similar to [19], to estimate the phase noise, a copy of the same oscillator was implemented with a common source buffer to take out the fundamental frequency. The fundamental signal at around 85 GHz has a high voltage swing and its phase noise can be measured from the buffer to be -97 dBc/Hz at 1 MHz offset. Because the third harmonic is used at the output, the estimated phase noise of the 256 GHz signal would be 9 dB higher than that of the fundamental. Hence, the estimated phase noise is around -88 dBc/Hz at 1 MHz offset. To measure the output power we used the same Erickson PM4 power meter as illustrated in Fig. 29(b). Output power of -19 dBm and -17 dBm was achieved at 256 GHz while consuming 38 mW and 71 mW of DC power, respectively. These values are around 12.6 dB lower than the simulated values. The main reason is that since the oscillator operates above the $f_{\max}$ of the transistors, the device models are not accurate. Table I compares this work with the state of the art. To the best of the authors'

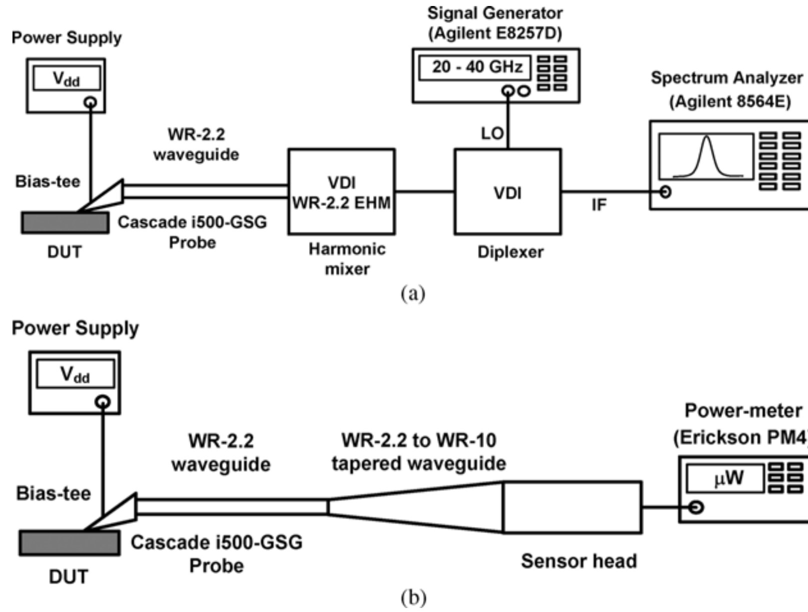


Fig. 29. Test setup for measuring (a) output frequency and (b) output power of the 482 GHz oscillator.

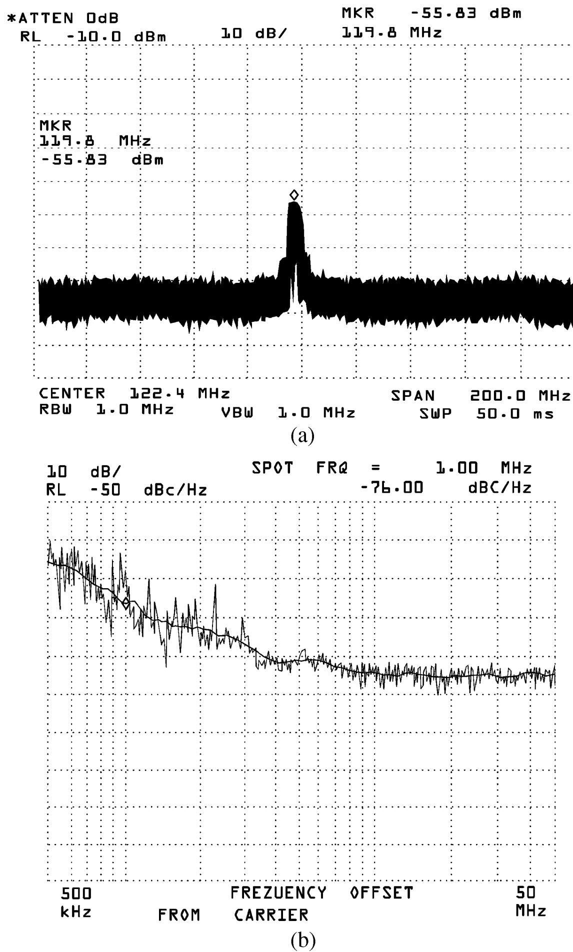


Fig. 30. (a) The measured IF spectrum of the 482 GHz signal for the 16th harmonic of the LO frequency when the power consumption is 35 mW from a 1.2 V supply and (b) its measured phase noise.

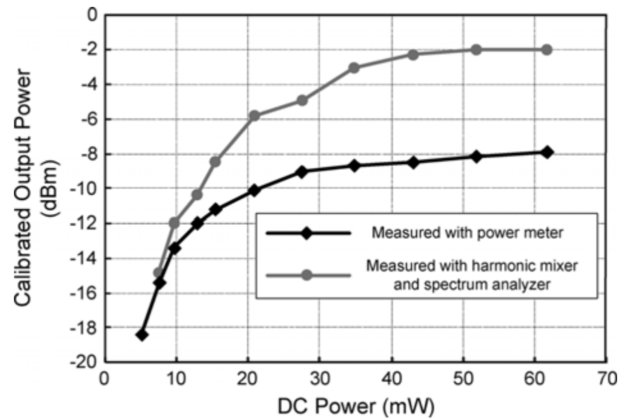


Fig. 31. The measured output power at 482 GHz as a function of DC power consumption.

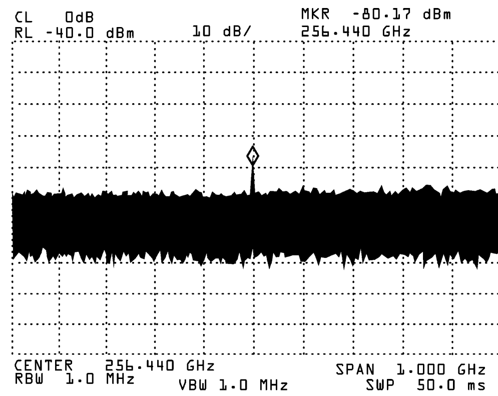


Fig. 32. The measured IF spectrum of the 256 GHz signal for the 48th harmonic of the LO frequency when the power consumption is 38 mW from a 1.25 V supply.

knowledge, this oscillator has the highest power reported in any CMOS or SiGe process in this frequency range and has the highest frequency reported in a 0.13 μm CMOS process.

VI. CONCLUSION

We have introduced a systematic method to design high power oscillators that can achieve frequencies close to the $f_{\max}$ of the transistors. We have also demonstrated a novel triple-push

TABLE I
COMPARISON WITH PRIOR ART

Ref.	Type	Technology	Frequency (GHz)	Power (dBm)	Phase Noise (dBc/Hz)	DC Power (mW)
[21]	Fundamental	90 nm CMOS	128	-37	-105 @ 10 MHz	9
[22]	Fundamental	90 nm CMOS	104	-8	NA	6.5
[24]	Fundamental	SiGe (f_{max}=300 GHz)	106	+2.7	-96.6 @ 1 MHz	337
[13]	Fundamental	InP (f_{max}=600 GHz)	254	-8	NA	11.7
[12]	Fundamental	InP (f_{max}=650 GHz)	346	-11	NA	115
[15]	Fundamental	InP (f_{max}=600 GHz)	330	-5.7	NA	15.8
[19]	Superposition	90 nm CMOS	324	-46	-91 @ 10 MHz (est.)	12
[20]	Push-push	45 nm CMOS	410	-47	NA	16.5
[36]	Push-push	0.13 µm CMOS	192	-20	-100 @ 10 MHz (est.)	16.5
[25]	Push-push	SiGe (f_{max}=275 GHz)	190	-4.5	-73 @ 1 MHz	215
[39]	Push-push	SiGe (f_{max}=275 GHz)	278	-25	NA	132
This work	Fundamental	0.13 µm CMOS	104	-2.7	-93.3 @ 1 MHz -105 @ 10 MHz	28
This work	Fundamental	0.13 µm CMOS	121	-3.5	-88 @ 1 MHz -102 @ 10 MHz	21
This work	Triple-push	0.13 µm CMOS	256	-17	-88 @ 1 MHz (est.)	71
This work	Triple-push	65 nm CMOS	482	-7.9	-76 @ 1 MHz	61
This work	Triple-push	65 nm CMOS	482	-9	-76 @ 1 MHz	27.5

structure to realize CMOS oscillators in the terahertz band. This approach has applications in millimeter-wave frequencies for communication and radar systems as well as terahertz band for bio- and molecular spectroscopy and imaging.

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