A Miniature 2 mW 4 bit 1.2 GS/s Delay-Line-Based ADC in 65 nm CMOS

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***Abstract*—A delay-line-based analog-to-digital converter for high-speed applications is introduced. The ADC converts the sampled input voltage to a delay that controls the propagation velocity of a digital pulse. The output digital code is generated based on the propagation length of the pulse in a fixed time window. The effects of quantization noise, jitter, and mismatch are discussed. We show that because of the averaging mechanism of the delay-line, this structure is more power efficient in the presence of noise and mismatch in deep sub-micron CMOS. To show the feasibility of this approach, a 4 bit 1.2 GS/s ADC is designed and fabricated in 65 nm CMOS in an active area of 110 μm$\times$ 105 μm. The measured INL and DNL of the ADC are below 0.8 bits and 0.5 bits and it achieves an SNDR of 20.4 dB at Nyquist rate. This delay-line-based ADC consumes 2 mW of power from a 1.2 V supply resulting in 196 fJ/conversion step without using any calibration or post-processing.**

***Index Terms*—Analog-to-digital converter, CMOS, delay-cell, delay-line, low-power, scaling, time-to-digital conversion.**

I. Introduction

HIGH-SPEED data conversion with modest resolution is used in high data-rate serial links and wideband wireless receivers [1]–[4]. Multiprocessor systems and multiband wireless receivers are two examples of such applications, where beside energy efficiency, area occupancy per ADC is also critical. In these applications it is desirable to have multiple channels on the same die in order a achieve the highest level of integration [5]–[7].

A diverse collection of voltage-based architectures ranging from flash to pipeline and successive approximation (SAR), with different variations has been reported for these low resolution, high-speed applications [1]–[4], [8]–[18]. In flash ADC, in order to achieve the highest sampling rate with the lowest power consumption, minimum size devices are normally used. However, using minimum size devices causes the highest amount of mismatch between individual comparators, which necessitates the use of calibration techniques. Background calibration is usually complex and imposes significant area and power overhead [8], [17]. On the other hand, foreground calibration requires periodic interruption of the ADC [9], [11], [12]. Alternatively, SAR ADC uses a single comparator and interleaves multiple cores to achieve a high sampling rate. In this case, calibration is still needed in order to match the gain and sampling phase of the parallel paths [15], [16]. In general, the underlying challenge in all of these architectures is that the voltage-based comparators are not scaled as favorably as digital circuits in CMOS. Although smaller CMOS gate lengths potentially enable faster sampling rates, mismatch still remains as a fundamental issue in analog circuits. As a result, voltage-based high-speed data converters are commonly accompanied with calibration.

Time-based signal processing has received much attention in applications such as digital phase-locked loops and time-of-flight measurements where a particular delay has to be accurately measured [19]–[24]. Vernier-based structures and time interpolation techniques are used to increase the time resolution beyond the minimum delay of a single cell [23]–[26]. Coarse-fine delay quantization is recently introduced to address the long length and difficult calibration required in single step structures [19], [20]. CMOS scaling has provided faster delay-cells, which is shown promising for time-to-digital quantization.

The concept of time-to-digital quantization can also be used in analog to digital conversion. In this case, the sampled input is translated into time domain and subsequently quantized using a delay-line structure. Previously such an ADC has been realized at low sampling rates [27]–[29]. VCO-based quantizers that use a ring oscillator and perform frequency-to-digital conversion have also been reported [30], [31]. In this work, we propose and demonstrate a novel time-based ADC that can operate at high data rates. We show how implementing the quantization process in time domain has distinct advantages compared to voltage domain quantization. Based on our proposed architecture we implement a 4 bit 1.2 GS/s delay-line based data converter with no calibration. This miniature ADC consumes less than 2 mW of power in only 0.01 mm^2 of active area. To the best of our knowledge, this is both the most compact and the most power efficient ADC, compared to high-speed data converters that do not rely on manual calibration.

The rest of the paper is organized as follows: Sections II and III explain the theory of the delay-line based ADC and the proposed architecture. Section IV describes the advantages of the delay-line based structure compared to voltage-mode quantization, and introduces a design methodology to decide which domain is more energy efficient for a given design specification and technology. Sections V and VI explain the implementation of the structure and the circuit level design followed by the measurement results.

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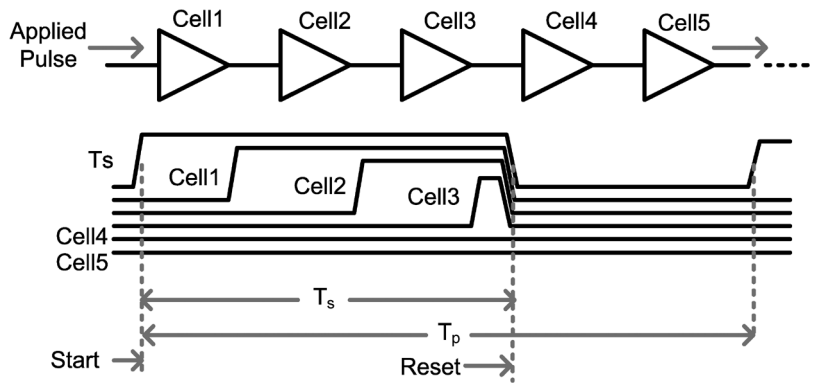

Fig. 1. A delay-line with a digital pulse applied to the first delay-cell. The propagation length of the pulse is quantized inside the delay-line through collecting the digital outputs of the delay-cells.

II. Delay-Line-Based Signal Quantization

Analog signals are not necessarily represented by voltage, and hence quantization is not necessarily made by voltage comparison. Contrary to comparator-based voltage quantization, in the delay-line-based quantizer a time that is proportional to the analog signal is quantized. A delay-line consisting of a series of delay-cells is shown in Fig. 1. A digital pulse is applied to the beginning of the delay-line and travels for a time window of T_s.

The delay-cell outputs are initially set to "0" and switch to "1" after the pulse propagates through them. At the end of the time window, T_s, the number of triggered delay-cells is the value of N that satisfies

$$\sum_{i=1}^{N} D_i < T_s < \sum_{i=1}^{N+1} D_i \tag{1}$$

where D_i is the delay of the i^{th} delay-cell. Here, we assumed that the line is long enough so that the pulse does not reach the end of the line during the time T_s. If this assumption is not valid, one can simply form a loop and take into account the number of rotations of the pulse.

For the simplest implementation, all delay-cells are assumed to have the same amount of delay equal to D. This results in N equal to

$$N = \left\lfloor \frac{T_s}{D} \right\rfloor. \tag{2}$$

This equation suggests that the process of time domain quantization can operate by either changing the time window or changing the amount of delay in each delay-cell [32]. These two methods result in two classes of time domain quantization which we call time-based quantization and delay-based quantization, respectively.

A. Time-Based Signal Quantization

In this technique delay-cells have a fixed delay and the time window is proportional to the input signal. Although this method is used in applications such as digital PLLs and time-of-flight measurement [19]–[24], it is not well suited for sampled mode circuits. This is because of the fact that systems operating with a fixed sampling rate need to have a fixed processing time in order to operate efficiently. Since the time window varies in the time-based quantizer, for small values of T_s, there will be significant idle time in the system. Nevertheless, this structure is quite suitable for data conversion in event-driven applications where the system is only expected to wake up when a new event arrives [33]. In these applications the delay-line operates only when a pulse arrives, while during the idle time it requires no DC current.

B. Delay-Based Signal Quantization

Alternatively, one can keep T_s constant and change the delay value of the delay-cells according to the analog input. Since T_s is fixed, this structure is advantageous for data converters. In most systems a sampled input is usually in the form of voltage or current. Assuming a voltage mode sampling, a delay adjustment block (DA) is required to apply the proper delay to the delay-cells based on the sampled voltage. The input-output relation from (2) becomes

$$N = \left\lfloor \frac{T_s}{D(v_{in})} \right\rfloor \tag{3}$$

where $D(v_{in})$ is the transfer function of the voltage-to-delay conversion and v_{in} is the sampled input voltage. If the DA generates an ideal delay relation as

$$D(v_{in}) = \eta / v_{in} \tag{4}$$

where η is constant, the quantizer output becomes a linear function of the input voltage

$$N = \left\lfloor \frac{T_s}{\eta} \cdot v_{in} \right\rfloor. \tag{5}$$

In other words, for the pulse propagation speed and the resulting quantized length to be proportional to the input, the delay of each cell should be inversely proportional to the input.

III. ADC Architecture

A. Delay-Cell Design

Variable delay-cells have been perviously implemented by various techniques such as current starved inverters and supply control [27], [34]. In order to maximize the quantizer's

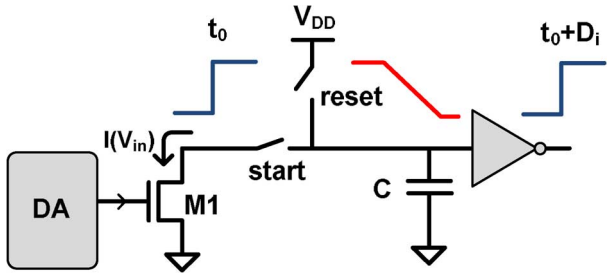

Fig. 2. The proposed controllable delay-cell. The current source linearly discharges the capacitive node when the start switch turns on by the previous stage. The delay-cell is reset to its high-level voltage at the end of the time window.

resolution, the delay-cell should maintain the relation in (4) for a wide range of input voltages. To achieve this, we propose the delay-cell shown in Fig. 2. A capacitive node is linearly discharged using a controllable current source, $M1$. The inverter succeeding the capacitor triggers at its switching threshold voltage, V_T [35]. The resulting delay value from the proposed circuit is

$$D(v_{in}) = \frac{C \cdot V_T}{I(v_{in})} + T_0 \tag{6}$$

where, C is the capacitance at the charging node, T_0 is the additional delay caused by the inverter and $I(v_{in})$ is the current of $M1$ which is linearly proportional to v_{in} through G_m, the transconductance of the DA. The delay offset caused by the inverter is a deviation from the ideal relation in (4), which limits both the dynamic range and the linearity of the delay-based quantizer. In order to minimize this effect, T_0 should be small compared to $D(v_{in})$. This criterion sets a lower limit on $D(v_{in})$. Assuming this lower limit is D_{min}, from (3) the maximum level of quantization becomes $N_{max} \leq T_s/D_{min}$. It is possible to increase N_{max} by increasing T_s, but this longer propagation time results in a lower sampling rate.

B. The Differential Delay-Line

To surmount the barrier caused by the inverter delay a differential delay-line is proposed. As shown in Fig. 3, a differential DA controls the delay of the two lines as a function of the sampled input, v_{in}. P-cells and N-cells in the two lines are similar, but their delay is set in a differential manner. This means that when P-cells are fast, N-cells are slow and vice-versa. First, we rewrite (6) as

$$D(v_{in}) = \frac{C \cdot V_T}{G_m(V_b + v_{in})} + T_0 \tag{7}$$

where G_m is the transconductance of the DA and V_b is a bias voltage. Since we are interested in the nonlinearity of the delay-line, we neglect any preceding nonlinearity caused by the sampling network and the DA, thus G_m is assumed to be constant. By defining the delay-line conversion gain G_D as

$$G_D = \frac{T_s G_m}{C \cdot V_T} \tag{8}$$

The quantized output for each of the two delay-lines becomes

$$N_P = \left\lfloor \frac{T_s}{\frac{C \cdot V_T}{G_m(V_b + v_{in})} + T_0} \right\rfloor = \frac{G_D(V_b + v_{in})}{1 + \frac{T_0}{T_s} \cdot G_D(V_b + v_{in})} - Q(N_P) \tag{9}$$

and

$$N_N = \left\lfloor \frac{T_s}{\frac{C \cdot V_T}{G_m(V_b - v_{in})} + T_0} \right\rfloor = q\frac{G_D(V_b - v_{in})}{1 + \frac{T_0}{T_s} \cdot G_D(V_b - v_{in})} - Q(N_N) \tag{10}$$

where $0 \leq Q(N) < 1$ represents the quantization error. N_P and N_N are the digital outputs of the P-cells and N-cells, respectively. Similar to the single delay-cell, (9) and (10) show that for a linear quantization the delay of the inverters should be small, i.e., $T_0 \ll D(v_{in})$. The differential output defined as $N_d = N_P - N_N$ equals to

$$N_d = \frac{2G_D v_{in}}{1 + 2\frac{T_0}{T_s}G_D V_b + \frac{T_0^2}{T_s^2}G_D^2\,(V_b^2 - v_{in}^2)} - Q(N_P) + Q(N_N). \tag{11}$$

Two important advantages of the differential delay-line compared to a regular delay-line can be observed from (11). First, the new quantizer conversion gain is $2G_D$, which means that the dynamic range is doubled compared to the single delay-line. Second, the signal dependent term in the denominator is of the second order which is significantly weaker than the first order terms in (9) and (10). Therefore, the differential delay-line provides both a higher dynamic range and a better linearity. The quantizer's input-output relation is plotted in Fig. 4 for the two cases.

C. Maximizing the Dynamic Range

In order to quantify the dynamic range, the quantization error should be derived. By neglecting the nonlinear components from (9) and (10), N_d can be written as

$$N_d = \lfloor G_D(V_b + v_{in}) \rfloor - \lfloor G_D(V_b - v_{in}) \rfloor . \tag{12}$$

Next, we separate the integer and non-integer parts so that $G_D V_b = n_b + r_b$ and $G_D v_{in} = n_i + r_i$, where n_b and n_i are integers and r_b and r_i are between 0 and 1. The resulting quantization error can be written as

$$Q_d = 2G_D v_{in} - N_d = 2r_i - \lfloor r_b + r_i \rfloor + \lfloor r_b - r_i \rfloor . \tag{13}$$

Assuming that the input is a uniform random signal, r_i becomes a uniformly distributed random signal between zero and one

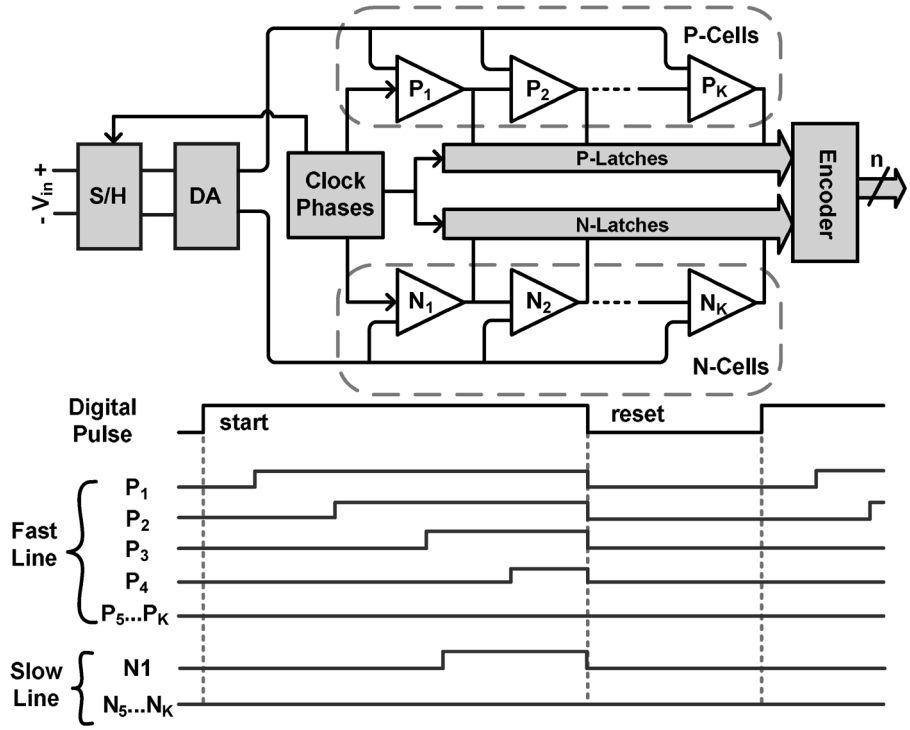

Fig. 3. The proposed differential delay-line based data converter. The input pulse is applied to both P-cells and N-cells and propagates in the two lines with different speeds. The outputs of P-cells and N-cells are latched separately and subsequently encoded as the digital output.

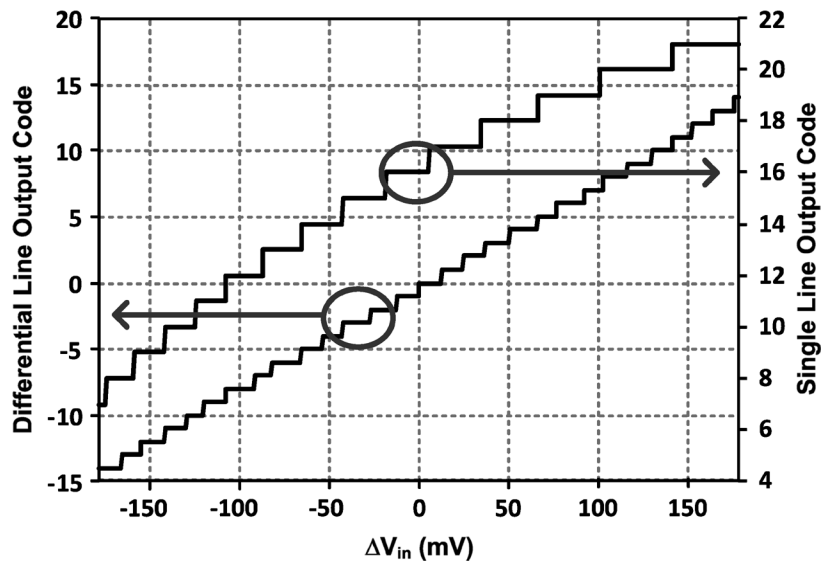

Fig. 4. Simulated input-output relation comparison between a single delay-line quantizer and a differential quantizer in the employed 65 nm CMOS process. The differential quantizer generates a higher dynamic range and linearity.

[36]. As shown in Fig. 5, the quantization noise expression in (13) has four regions separated based on r_b and r_i:

$$Q_d = \begin{cases} 2r_i, & r_b < 1 - r_i,\ r_b > r_i \\ 2r_i - 1, & r_b > 1 - r_i,\ r_b > r_i \\ 2r_i - 1, & r_b < 1 - r_i,\ r_b < r_i \\ 2r_i - 2, & r_b > 1 - r_i,\ r_b < r_i. \end{cases} \tag{14}$$

From (14), it can be shown that the average of the quantization noise is zero, i.e., $\overline{Q_d} = 0$. Consequently, by applying its definition, the quantization noise variance can be computed from (14):

$$\sigma_Q^2 = \int_0^1 (Q_d - \overline{Q_d})^2 \cdot dr_i$$

$$\sigma_Q^2 = 1/3 - 2|r_b - 0.5| + 4(r_b - 0.5)^2. \tag{15}$$

Equation (15) shows that the optimal bias point that corresponds to $r_b = 1/4$ or $r_b = 3/4$ results in minimum value

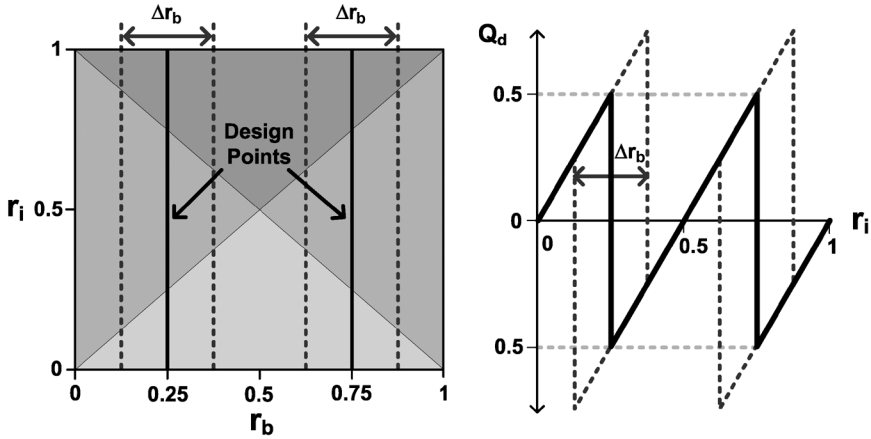

Fig. 5. Left: the quantization error separated to different regions based on the bias point. Right: the noise variance corresponding to sub-optimal and optimal bias points.

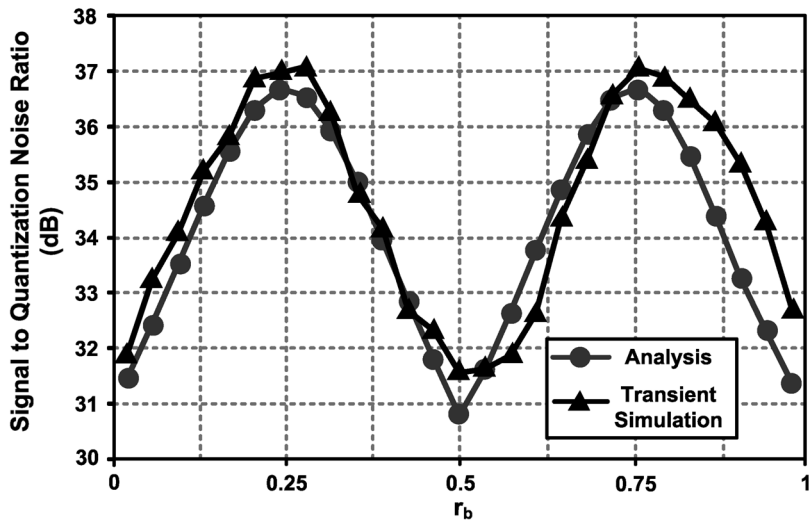

Fig. 6. Signal to quantization noise ratio as a function of the bias point from theoretical analysis of the differential delay-line compared to the simulation results from the time domain spectrum in the employed 65 nm CMOS process.

of $\sigma_Q^2 = 1/12$. Fig. 5 shows the bias regions and compares the quantization noise for optimal and sub-optimal bias points. The signal-to-noise ratio from this analysis is compared with the result from time-domain response of the delay-line in Fig. 6, which shows a reasonable match.

By combining (15) and (12), the dynamic range of the differential quantizer becomes

$$DR = \frac{\overline{N_d^2}}{\sigma_Q^2} = 6(G_D v_{max})^2 \tag{16}$$

where v_{max} is the maximum range of the input voltage. Since in reality, the dynamic range of the delay-cell is the actual limit, it is useful to rewrite (16) in terms of the minimum delay. By substituting (8) and (7) into (16) we get

$$DR = \frac{\overline{N_d^2}}{\sigma_Q^2} = 6\left(\frac{T_s}{D_{min}}\right)^2 \tag{17}$$

where D_{min} is the minimum delay corresponding to v_{max} and is a property of the process. By defining N_{max} as the output corresponding to the minimum delay D_{min}, the dynamic range equals to

$$DR = 6(N_{max})^2. \tag{18}$$

For a fixed sampling rate, N_{max} provides a useful benchmark to evaluate how various properties of the delay-line-based structure enhance with scaling. From (18), doubling the delay speed or the time window, results in one additional bit.

IV. Non-Ideal Effects

A. Time-Domain Averaging

Consider a delay-line consisting of similar delay-cells. All the nonideal effects of the i^{th} delay-cell can be combined into an input referred delay error, d_i, followed by an ideal delay-cell with a delay equal to $D(v_{in})$. We assume d_i has a Gaussian distribution with zero mean and standard deviation of σ_d. The governing equation from (1) in the presence of errors becomes

$$N \cdot D(v_{in}) + \sum_{i=1}^{N} d_i < T_s < (N+1) \cdot D(v_{in}) + \sum_{i=1}^{N+1} d_i \cdot \tag{19}$$

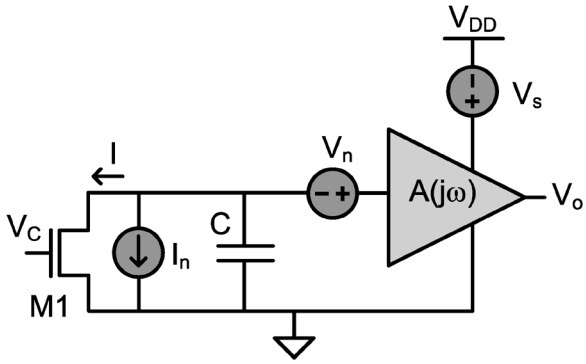

Fig. 7. Sources of noise and jitter in the delay-cell.

This means that N is a random variable whose standard deviation represents the output error. For this analysis we neglect the effect of quantization error. We also assume that the error of each delay-cell is much smaller than its delay, i.e., $\sigma_d \ll D(v_{in})$. With these assumptions, (19) can be written as

$$N = \frac{T_s - \sum_{i=1}^{N} d_i}{D(v_{in})}. \tag{20}$$

By taking the variance of both sides, we arrive at

$$\sigma_N^2 = \frac{N\sigma_d^2}{D(v_{in})^2}. \tag{21}$$

By following the analysis similar to Section III, we can obtain the signal-to-error ratio (SER) as

$$SER = \frac{\overline{N_d^2}}{\sigma_{N\,max}^2} = \frac{1}{2} N_{max} \left(\frac{D_{min}}{\sigma_d}\right)^2. \tag{22}$$

Note that (22) assumes N_{max}, where delay-cells have their minimum value D_{min}. From (21), this value causes the highest output noise which is a lower bound for SER.

A curious result of this analysis is that the delay-line inherently averages out the error contribution from the individual cells. As a result a longer delay-line corresponding to a higher N_{max} results in a higher signal to error ratio. This averaging effect is a distinct feature of the delay-based quantization. In the following, we use this analysis to determine the effects of noise and mismatch on this quantizer.

B. Noise and Jitter

The two major noise sources in a delay-line are the device noise and supply noise. In Fig. 7, the charging node is followed by an inverter. For noise analysis, the small signal model of the inverter which is a first order amplifier with a gain of A_0 and the unity gain cut-off frequency of ω_0 can be used. The input referred noise of the amplifier and the current noise of $M1$ are represented by V_n and I_n, and the supply noise is represented by V_s. The time domain response of the delay-cell in the linear region without noise sources becomes

$$V_o(t) = \frac{A_0 I}{C} \cdot \left(t - \frac{e^{-\omega_0 t} - 1}{\omega_0}\right). \tag{23}$$

According to (23), with the typical parameter values, the time response of the inverter is much faster than the overall delay. This means that the noise of the previous delay-cell only changes the trigger time but has negligible effect on the noise of the following cell. Hence, the delay variance can be estimated based on the time the inverter reaches V_T. By referring all noises to the input of the inverter, we have

$$\begin{aligned} D_n &= \frac{C}{I} \cdot \left(V_T - V_n - V_s - \frac{1}{C}\int_0^D I_n \cdot dt\right) \\ \sigma_n^2 &= \left(\frac{C}{I}\right)^2 \cdot \left(\sigma_{V_n}^2 + \frac{D}{C^2} \cdot I_n^2 + \sigma_{V_s}^2\right) \\ &= \left(\frac{C}{I}\right)^2 \cdot \left(\sigma_{V_{dn}}^2 + \sigma_{V_s}^2\right) \end{aligned} \tag{24}$$

where D_n is the delay in the presence of noise, σ_n^2 is the jitter of a single delay-cell, and $\sigma_{V_{dn}}^2$ represents the total device noise. Hence, the jitter consists of two components: The first component is due to the noise of the inverter and the current source and the second component comes from all externally induced noises, most importantly the supply noise.

In the differential delay-line scheme, the supply noise affects both sides equally when the noise bandwidth is low compared to the sampling rate. Thus, when high frequency components are sufficiently filtered, the differential structure cancels out the effect of the supply noise on jitter. Moreover, the device noise sources are independent across the delay-line, hence by substituting (24) into (21) and neglecting T_0, the signal to noise ratio equals to

$$SNR = \frac{1}{2} \cdot \frac{V_T^2}{\sigma_{V_{dn}}^2} \cdot N_{max}. \tag{25}$$

As a direct result of averaging, SNR increases by increasing the number of delay-cells. This means that a faster process results in a higher N_{max}, increasing the SNR of this quantizer.

C. Mismatch

Mismatch between delay-cells comes from random variations in device dimensions and the threshold voltage [10]. From (7), variation in either of these parameters affects the delay value. By calculating σ_d from (7) and substituting into (22), the signal-to-error ratio becomes

$$SER = \frac{1}{2} \cdot \frac{N_{max}}{\left(\frac{\sigma_{V_T}}{V_T}\right)^2 + \left(\frac{\sigma_C}{C}\right)^2 + \left(\frac{\sigma_{G_m}}{G_m}\right)^2} \tag{26}$$

where σ_{V_T}, σ_C, and σ_{G_m} are the variations of the threshold voltage, charging capacitor, and G_m, respectively. The terms in the denominator of (26) depend on process properties. The last term in the denominator also depends on the bias point and is represented by its average value. Equation (26) shows that the effect of mismatch in a sufficiently long delay-based quantizer is less than a comparator-based quantizer. For instance, in a calibration-free flash ADC, for an input voltage range of V_{swing}, the ratio σ_{V_T}/V_{swing} should be smaller than the LSB. However,

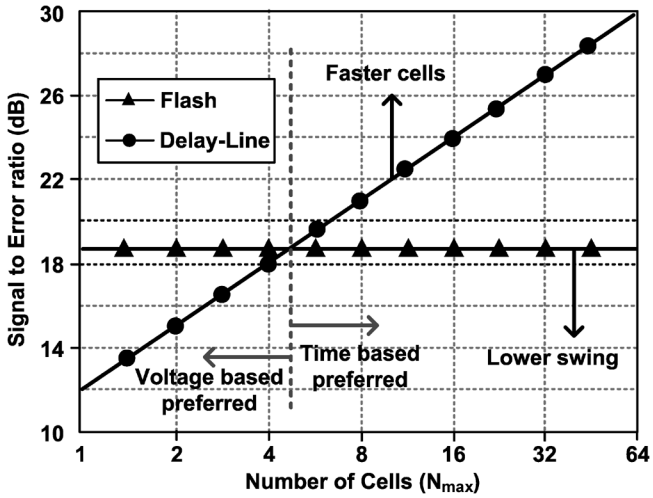

Fig. 8. Comparison of mismatch limited signal-to-noise ratio between basic flash and the delay-line structure. Monte-Carlo simulation is performed for the 65 nm process and the SER is calculated assuming similar input voltage range. The horizontal arrows indicate the regions in which each structure is favorable. The vertical arrows indicate the direction of further scaling which is in favor of the delay-line structure.

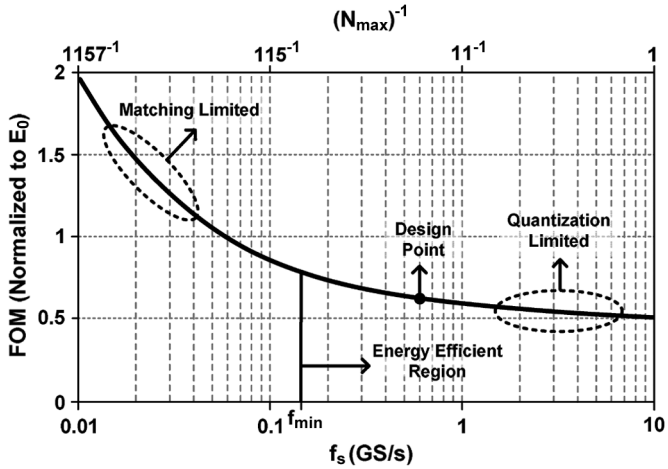

Fig. 9. FOM as a function of sampling rate and resolution for the used 65 nm CMOS process. The selected sampling frequency is shown with the dashed line. Above f_{min} the delay-line is in the quantization limited region where sampling rate can be traded for higher resolution while maintaining minimum energy consumption per bit.

in the delay-line structure because of the mismatch averaging, this ratio is relaxed by a factor of $\sqrt{N_{max}}$.

Fig. 8 compares the mismatch-limited SER for flash and the delay-line-based structure based on Monte-Carlo analysis in a 65 nm CMOS process. For a fair comparison, the device sizes and input voltage swings are set to be equal. As a result of mismatch averaging, the delay-line is advantageous above a certain number of cells. As indicated in Fig. 8, the intersection between the two plots also scales, as faster devices move the delay-line to higher SERs and lower supply voltages move the SER of flash structures further down. As as a result, the delay-line based structure is favorable for deep sub-micron CMOS scaling.

D. Design Methodology

In order to find the optimal number of delay-cells, the energy efficiency for the ADC should be evaluated using the figure-of-merit [13]

$$FOM = \frac{P}{2^{ENOB} \cdot f_s} = \frac{E_D}{\left(\frac{2}{3} \cdot SNDR\right)^{1/2}} \tag{27}$$

where E_D is the energy consumed per conversion. The power consumption during pulse propagation comes from the charging of the delay-cells most of which is consumed for charging the capacitive node of the delay-cells. The energy per transition in a delay-cell defined as E_0, is equal to $CV_{dd}^2/2$ which is constant. As a result the energy consumption in the delay-line becomes

$$E_D = E_0 \cdot (N_P + N_N) = E_0 \cdot N_{max} \tag{28}$$

where N_P and N_N are replaced from (9) and (10). According to simulation, for the target number of bits (4–6 bits) mismatch and quantization noise are the dominant sources of error and the effect of the jitter induced by the device noise is negligible. Using this result and by substituting (18) and (22) into (27), energy per conversion step becomes

$$\begin{aligned} FOM &= E_D \cdot \left[\frac{3}{2} \cdot (DR^{-1} + SER^{-1})\right]^{1/2} \\ &= \frac{E_0}{2} \cdot \left(1 + \frac{12\sigma_d^2}{f_s \cdot D_{min}^3}\right)^{1/2}, \end{aligned} \tag{29}$$

where $f_s = T_s^{-1}$ is the highest possible sampling rate. Fig. 9 shows the variation of FOM in the employed 65 nm process as a function of the sampling frequency. At high frequencies, the delay-line has a constant FOM limited by the quantization noise. In this range, the delay-line-based ADC can have a variable sampling rate with a fixed energy efficiency. At lower frequencies, the effect of mismatch increases the required energy per bit. Thus, it is desirable to design the ADC above the knee of this curve which can be calculated from (29) as

$$f_{min} = \frac{12\sigma_d^2}{D_{min}^3}. \tag{30}$$

From (30), f_{min} will significantly increase for faster processes which results in a higher resolution in the low-power region. In this design, the knee frequency is $f_{min} = 140$ MS/s and we choose the sampling rate of $f_s = 600$ MS/s which is well above the f_{min}. This sampling rate also provides an N_{max} which is high enough for a 4 bit quantizer.

V. Circuit Design

To show the feasibility of the proposed approach, we design and simulate a 4 bit 600 MS/s ADC on a standard 65 nm CMOS process. Next, two of these core ADC's are time-interleaved to achieve the sampling rate of 1.2 GS/s. In this section, we discuss the key circuit blocks of the core delay-line-based ADC.

A. Sample and Hold

In most applications, the input signal is in the form of voltage or current. In order to use the concept of delay-based quantiza-

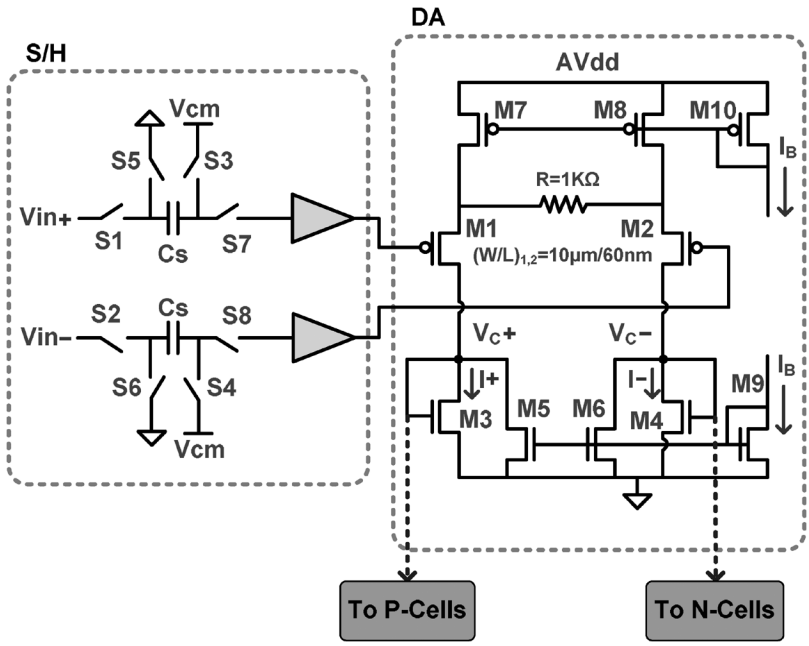

Fig. 10. Input sampling switches and the delay adjustment circuit.

tion in these applications, a voltage-mode sampling circuit is designed. The front-end switching network is shown in Fig. 10. The input uses all-NMOS transistors that operate with two non-overlapping phases.

For best performance, the RC time constant of the switching network should be small compared to the period of the input signal. Hence, larger switches $(S1 - S8)$ and a smaller sampling capacitor (Cs) are desired. A small capacitor is also advantageous to reduce the loading effect on the prior stage. However, the capacitor needs to be sufficiently large to store enough charge during the hold phase. In this design, simulation shows that $Cs = 25$ fF meets the requirement for this frequency and resolution. In addition, the maximum tolerable switching charge injection sets the upper limit on the size of the switches.

The common mode voltage is set to $Vcm = 300$ mV as it should be low for the best linearity in the switches but high enough for the switching network to have acceptable voltage swing. A source follower acts as a buffer stage between the sampling circuit and the differential pair. The buffer reduces the amount of charge loss in the sampling network, allowing a smaller sampling capacitor. Therefore, adding the buffer enables a faster sampling network for a given resolution.

B. Delay Adjustment Circuit

Delay adjustment as shown in Fig. 10 operates using a degenerated differential pair composed of $M1$ and $M2$. During the hold phase, the sampling capacitors are connected to the differential pair and the differential input voltage is transformed into a differential current in $M3$ and $M4$. PMOS transistors are selected as the input differential pair to lower the bias voltage of the preceding switches. Also this allows the load to be NMOS, resulting in a faster settling time and faster deley-cells. The transconductance gain of the differential pair, equals to $g_{in}/(2+g_{in}R)$, where g_{in} is the transconductance of $M1$ and $M2$ and R is the degeneration resistor. Because of the separating buffer, the input transistors can be designed sufficiently large to ensure $g_{in}R \gg 1$ across the entire input range, resulting in minimal variation in G_m.

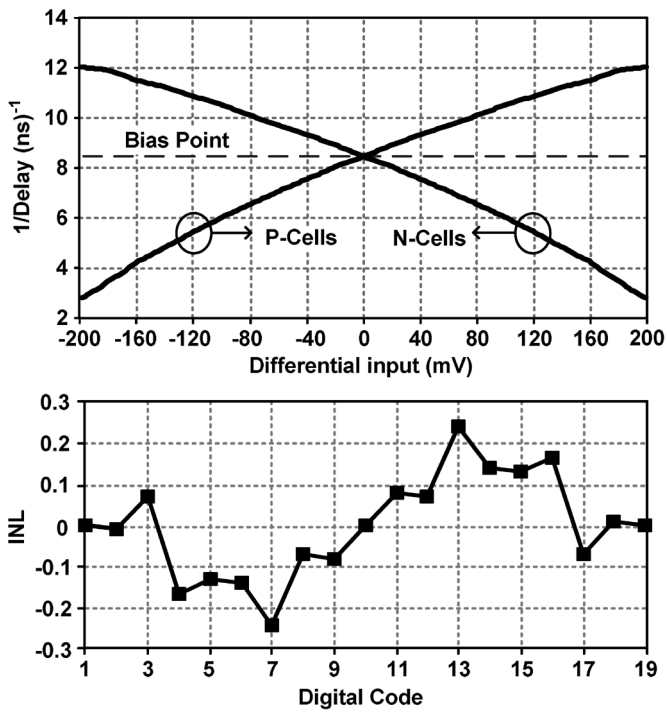

Fig. 11. Top: transfer function of the input voltage to the inverse delay. The dashed line represents the bias point of the delay-cells. Bottom: INL of the resulting differential quantizer.

The bias current of $M3$ and $M4$ is set based on the difference between the NMOS and PMOS current sources ($M9$ and $M10$). These two current sources copy the same bias current with different ratios based on their respective sizes. This bias current is important for two reasons. First, since the delay-cells consume

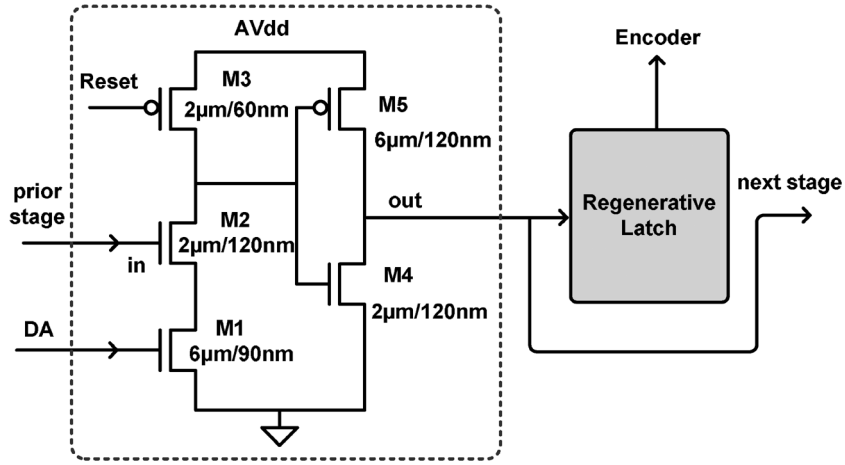

Fig. 12. Delay-cell followed by the latch. The delay-cell is triggered by the previous stage but all delay-cells are reset at the same time.

power only during the transitions, the differential pair is the only circuit that draws DC current. This means that lowering the bias current decreases the overall power consumption. However, the bias current has a lower bound which is set by the required settling time of the DA. Second, the bias current determines V_b in (7) which should be set to minimize the differential quantization error, Q_d. Since this minimum error occurs for several optimal bias points, both of these optimizations can be achieved simultaneously. The inverse delay as a function of the input voltage for both P-cells and N-cells and the nonlinearity resulting from the nonideal input-output relation is plotted in Fig. 11.

C. The Delay-Cell

Fig. 12 shows the circuit realization of the delay-cell proposed in Section III-A. $M1$ acts as an adjustable current source and its current is set by DA transistors $M3$ and $M4$ for P-cells and N-cells, respectively. $M2$ is an NMOS switch and is triggered by the pulse from the prior stage. The succeeding inverter consisting of $M4$ and $M5$ provides the capacitance of the charging node of the delay-cell.

The operation of the delay-cell has two phases. During the pulse propagation when the pulse arrives at the gate of $M2$, this switch turns on and the current source starts discharging the capacitive node from AV_{DD} to ground. Eventually the inverter flips and its output is applied to the next delay-cell. At the end of the time window, T_s, the output of the inverter is latched and the capacitive node is reset by $M3$. In other words, the delay-cells are charged sequentially, but their outputs are all latched and reset at the same time to record the quantized output for the current sample.

Since the capacitive node is floating during pulse propagation, we should consider the charge leakage. This charge leakage can change the characteristic of the delay-cell and introduce nonlinearity. In order to minimize this effect, both M1 and M2 have gate lengths above the minimum length and their subthreshold current is ensured to be small compared to the saturation current of M1 during discharge. In this design, the amount of charge leakage during the pulse propagation time has negligible effect on the ADC performance.

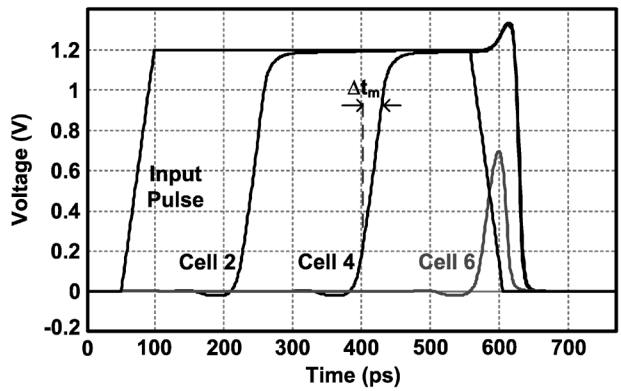

Fig. 13. Time response of the delay-line outputs. If a cell is latched during the transition time $\triangle t_m$, the resulting bit is not clear. The uncertainty is kept below noise floor by ensuring sharp transitions for the delay-cells.

The regenerative latch at the output of each delay-cell is optimized for low-power and high-speed operation. For a more reliable timing scheme, a master-slave topology is used [35]. In order to minimize the loading effect and the switching noise of the latch, we place a buffer between the latch and the delay-cell. The resulting output of each delay-cell is a single bit. The output bits from all delay-cells are connected to a digital encoder to generate the final digital code.

Using a regenerative latch brings the concern of metastability [35]. A latch requires a minimum setup time and hold time in order to function properly. The delay-cell outputs are high or low for most of the time. However, as shown in Fig. 13, there is a chance of metastability if the time window T_s ends when a delay-cell is in transition. In this case the final latched value is decided mainly by noise. The resulting uncertainty in the output of one delay-cell across the delay-line adds to the overall quantization error. In order to minimize the effect of metastability, the transition time of the delay-cell should be small compared to the minimum delay value, D_{min}. This is ensured by the output inverter which makes sharp transitions. In our design, the transition time is around 40 ps which is smaller than the D_{min} of 80 ps. Compared to voltage comparators where preamplification is necessary to overcome the latching uncertainty, delay-line based

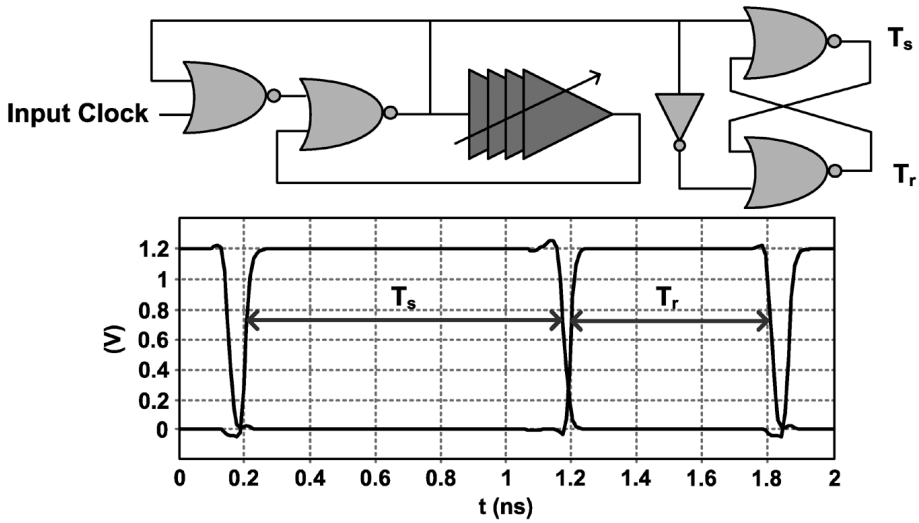

Fig. 14. Edge triggered pulse generator (top), and the two generated phases (bottom). The delay-cells are similar to the core delay-cells to ensure robustness to temperature and process variations.

quantization has the advantage of being robust to this kind of error especially in faster processes.

D. Clock Phase Generator

The ADC operates in two non-overlapping clock phases. During the first phase with the time window of T_s, the sample and hold tracks the input voltage. At the same time, the pervious sample is applied to the delay-cells and the pulse propagates through the delay-line. At the second phase with a time length of T_r, the sampled input sets the current of $M3$ and $M4$ in the DA as shown in Fig. 10. Also during this phase the output of the delay-cells are latched and they reset.

To optimize the FOM of the ADC, we have to carefully select the ratio of T_s and T_r. As discussed in Section IV-D and Fig. 9, for the best FOM, the ADC operates in the quantization noise limit, which means that resolution is a linear function of T_s. As a result, for the highest resolution, the larger portion of the period should be dedicated to this phase. The remaining time in each period is T_r, which is determined by the settling time of the DA. However, a DA with shorter settling time increases the power consumption. Hence, T_r should be long enough to keep the power consumption of the DA low compared to the entire ADC.

The absolute delay of each cell is sensitive both to temperature and process variations. In the differential structure, these variations happen in common mode. Variation in the common mode of the delay-line changes the bias point, causing suboptimal performance. The solution of this problem lies in the fact that the quantized output is a function of the ratio $T_s/D(v_{in})$. Thus, if T_s changes proportional to $D(v_{in})$, the resulting ratio becomes robust to variations. To implement this, an edge triggered pulse generator is used as shown in Fig. 14. The input pulse triggers a delay-line and the output of the delay-line produces a time window equal to the total delay of the line. The delay-line produces T_s and the following logic generates two non-overlapping phases. The delay-line in the pulse generator uses delay-cells similar to the core delay-cells. As a result, the pulse length (T_s) varies proportional to the absolute delay of the cells $(D(v_{in}))$. Fig. 15 shows the simulated variation in the delay-line output for the employed technique compared with using a fixed time window. ΔN_{max} is defined as the difference between N_{max} at a certain process/temperature with its value at TT. Fig. 15 demonstrates that using the proposed adaptive time window, ΔN_{max} remains below 1 LSB while a similar quantizer with a fixed time window is more sensitive to process/temperature variations.

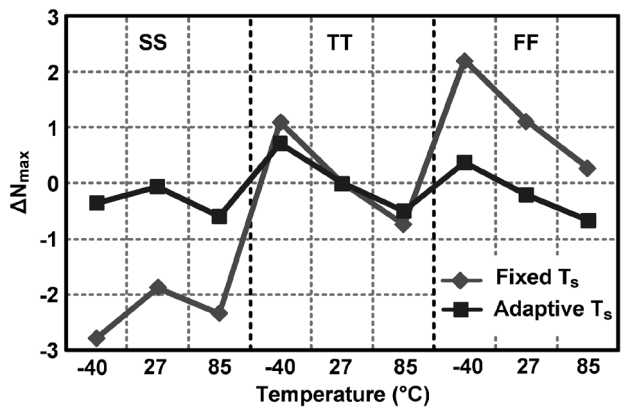

Fig. 15. The effect of process and temperature variation in the delay-line for the employed adaptive pulse width technique compared with using a fixed pulse width.

VI. Prototype Measurement

The proposed ADC is fabricated in a 65 nm CMOS process. To have 4 bits, each delay-line consists of 8 delay-cells followed by a dummy cell at the end. The ADC including the digital section occupies an active area of only $110\ \mu\text{m} \times 50\ \mu\text{m}$. The miniature size of this structure is a direct result of using delay-line quantization instead of comparators. The small size of the delay-line also helps in avoiding global variations on chip. As a result, cell to cell variations maintain similar statistical properties, which is required for effective averaging. The fabricated chip includes 16 cores that can operate independently or together in a time interleaved fashion. In the time interleaving

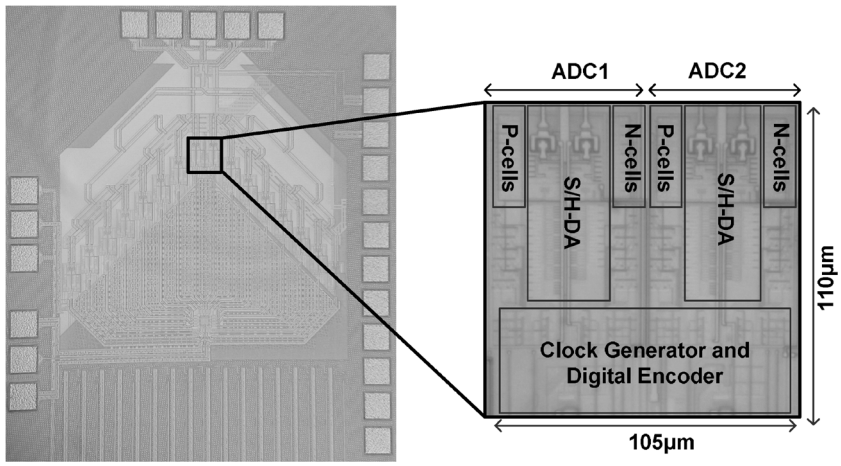

Fig. 16. Chip photograph.

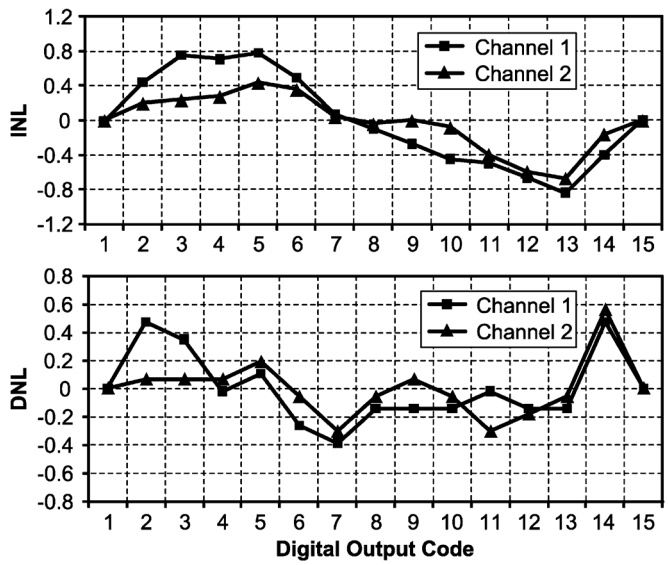

Fig. 17. Measured INL (top) and DNL (bottom) of the two channels.

TABLE I
PERFORMANCE SUMMARY

Technology	TSMC 65nm CMOS
Resolution	4 bits
Sampling Rate	1.2 GS/s
Power Supply	1.2V
Input Range @ Nyquist	600 mV (pp-diff)
Power Consumption	2 mW
Number of Channels	2
DNL	+0.54LSB/-0.38LSB
INL	+0.78LSB/-0.83LSB
SNDR @ f_{in}=602MHz	20.4 dB (23.1 dB peak)
SFDR @ f_{in}=602MHz	30.1 dB (33.2 dB peak)
Input Capacitance	50 fF
Active Area	105μm×110μm

mode, the input clock at 9.6 GHz, is divided into 16 phases for each core. This results in a sampling rate of 600 MS/s for each core. In this design, only two channels are interleaved in order to avoid the need for mismatch and clock-skew calibration for the target resolution. Multiple chip measurements have confirmed that these two channels can be reliably interleaved without any calibration. The analog input and the clock are applied using RF probes and a differential buffer connects the analog input to the cores.

The resulting two core delay-line ADC operates with a sampling rate of 1.2 GS/s. The measured data corresponds to $T_r = 610$ ps and $T_s = 970$ ps. Both cores have the same time window and share the same bias current for the DA which is applied externally. The chip photograph with individual blocks is shown in Fig. 16. Most of the core area is covered by the sample-and-hold circuit and the digital interface. The INL and DNL of the two channels plotted in Fig. 17 are below 0.8 LSB and 0.5 LSB, respectively. The Nonlinearity in the INL curve is mostly deterministic. This suggests that the resolution is limited by nonideal characteristic of the delay-cells, not by device mismatch. This is expected from Fig. 9, as our target resolution is lower than the maximum achievable N_{max} for this sampling frequency. As a result, by using smaller delay cells and a nonuniform delay-line, the deterministic nonlinearity can be compensated and a higher dynamic range is possible.

At high input frequencies, the limited bandwidth of the sampling switches and buffers, lowers the voltage to delay conversion gain. As a result, the differential input range has to be increased in order to maintain full scale quantization. Since nonlinearity is not limited by the input buffers or switches, this increase does not affect the overall linearity of the ADC. High frequency measurement is done both by sweeping the input frequency up to the Nyquist rate and by sweeping the sampling frequency up to 1.2 GHz. The measurement results are shown in Fig. 18. The SNDR remains above 20.4 dB and the SFDR remains above 29.23 dB for the entire range. The measured output spectrum is plotted in Fig. 19.

The total power consumption of the two-core ADC excluding the buffers is 2 mW. The share of the sample-and-hold and the DA is 480 μW per channel and the core delay-line consumes 520 μW per channel. From the analysis in Section IV-D, the

TABLE II
PERFORMANCE COMPARISON OF STATE-OF-THE-ART ADCS

Ref.	Architecture	Technology	bits	f_s (GS/s)	Power (mW)	Calibration	Area (mm^2)	FOM (pJ/Step)
[9]	Flash	180nm	4	4	78	Foreground	0.88	4.3
[11]	Folding-Flash	65nm	5	1.75	2.2	Foreground	0.02	0.050
[14]	SAR	65nm	6	1	6.7	Foreground	0.11	0.210
[8]	Folding-Flash	90nm	6	2.7	50	Background	0.36	0.470
[17]	SAR	130nm	6	1.25	32	Background	0.09	0.785
[15]	SAR	65nm	5	0.25	1.2	Redundancy	5	0.240
[3]	Flash	90nm	4	2	10	None	0.55	0.361
[10]	Flash	130nm	6	1.6	180	None	0.42	2.6
[13]	Two-step Flash	130nm	6	1	49	None	0.16	1.24
This Work	**Delay-Line**	**65nm**	**4**	**1.2**	**2**	**None**	**0.01**	**0.196**

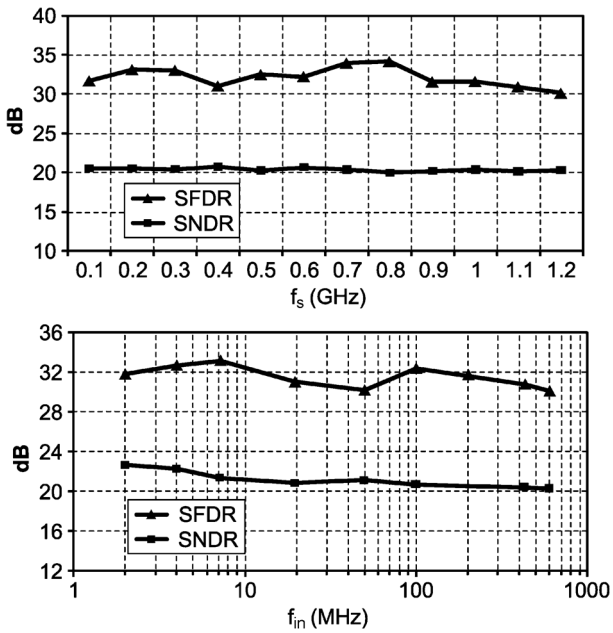

Fig. 18. Top: measured SFDR and SNDR at Nyquist rate vs. sampling rate. Bottom: measured SFDR and SNDR versus input frequency at $f_s = 1.2$ GS/s.

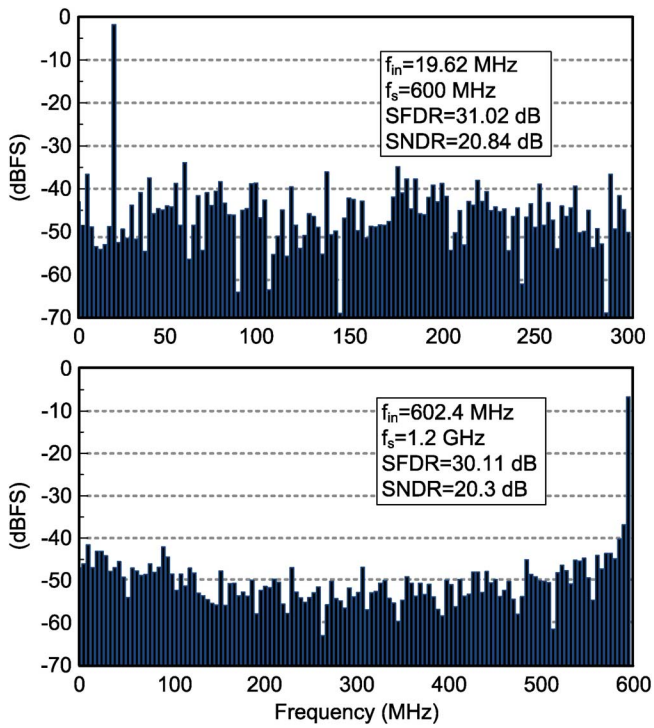

Fig. 19. Top: measured low frequency spectrum for one channel. Bottom: measured Nyquist rate output spectrum, when both channels are interleaved.

power consumption of the delay-line is expected to further reduce in faster processes. The supply of the delay-line is separated and decoupled to minimize jitter. Low frequency ENOB is 3.6, and at the highest sampling rate the ENOB is equal to 3.1, which results in a FOM equal to 196 fJ/Step. The performance of the ADC is summarized in Table I. As shown in Table II, this ADC provides the highest energy efficiency among ADCs in this frequency range that do not rely on foreground calibration. Moreover, the active area of the two-core ADC is 0.01 mm^2, which is remarkably small compared to conventional ADCs with or without calibration.

VII. CONCLUSION

A delay-line-based data converter is introduced for high-speed and low-power applications. The sampled signal is transformed into time-domain and subsequently quantized using a differential delay-line. We illustrate how the proposed structure is advantageous in deep-submicron technology compared to voltage-based data converters. To verify the concept, a prototype chip is fabricated and measured in 65 nm CMOS. Compared to other calibration-free ADCs in the same frequency and resolution range, the proposed ADC is more power efficient and compact.

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