2-D Electrical Interferometer: A Novel High-Speed Quantizer

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***Abstract*—In this paper, we propose a 2-D electircal interferometer as a means of high-speed data conversion. The structure is based on wave propagation in 2-D LC lattices. We will discuss the principle behind this technique, which exploits wave propagation and medium manipulation in order to take advantage of different interference patterns. This method of quantization is based on passive LC lattices that can operate at very high frequencies on a conventional CMOS process. We analyze different properties of the structure and propose the design methodology. To show the feasibility of this approach, we design a 20-GS/s 4-bit quantizer consuming 194 mW for quanization and 943 mW for an analog memory. There is good agreement between analysis and simulation.**

***Index Terms*—Analog-to-digital converter (ADC), CMOS, interference, LC lattice, power detector, quantization, tapering, wave propagation.**

I. Introduction

THE GROWING demand for higher data rates is increasing attention paid to extremely fast signal quantization. The applications include equalization and detection in serial data links, wideband radar and RF receivers, and high-speed instrumentations [1]–[9]. High-speed data conversion faces different challenges both in the fundamental aspect due to limited active device cutoff frequency and in implementation aspects due to issues such as sampling jitter and clock/data skew [6]. The fastest reported quantizers use high-performance compound-semiconductor processes and/or time interleaving to go beyond the speed limit of a single-channel data converter. However, clock jitter and channel mismatch remain as the main challenges of the time-interleaving approach [3]–[7]. To address the issue of sampling jitter, optically assisted sampling has been proposed, which can lower the jitter noise floor while increasing the fabrication cost [5], [11].

Although conventionally analog signals are converted from voltage or current domain directly to the digital domain, it is not necessarily the most effective method because of active device limitations. In [10], time stretching in an optical medium is proposed for fast quantization. In [11] and [12], optical sampling/quantization using optical phase shifters and power detectors has been proposed as another alternative for achieving higher sampling rates. In our previous work, we proposed the delay-line-based quantization, which exploits CMOS fast delay cells for GSample/s and power-efficient data conversion [13], [14].

In this paper, we will propose wave propagation in electrical lattices as another means of signal quantization that can be used for extremely high-speed data conversion on silicon. 1-D and 2-D LC lattices have been previously studied and exploited in extremely high-speed signal generation and transmission [15]–[21]. Another area in which LC lattices have shown promising potential is fast signal processing [22]–[27]. Wave propagation in discrete lattices is shown to behave similarly to a continuum media provided the wavelength is considerably larger than one lattice spacing. In this region of operation, 2-D lattices behave similarly to an optical medium, and properties such as diffraction and refraction are observed [24]–[26].

The general idea of using an LC lattice as a quantizer is portrayed in Fig. 1. The analog signal changes the properties of the medium, which will in turn change the interference pattern inside the wave-propagating medium. The properties of the wave can be changed by using varactors in the LC lattice and controlling their bias points. Furthermore, we can engineer the values of inductors and capacitors at different points of the lattice to generate the desirable interference pattern. Since this kind of change in lattice properties does not involve any signal processing with active devices, it is inherently fast. Another way to describe the process is that the analog signal is spread across the entire lattice, making it a spatial quantizer. To the best of our knowledge, this is the first structure that quantizes the analog signal in a 2-D electrical lattice. Depending upon the way the LC lattice is designed, certain nodes in the lattice become more vital for signal

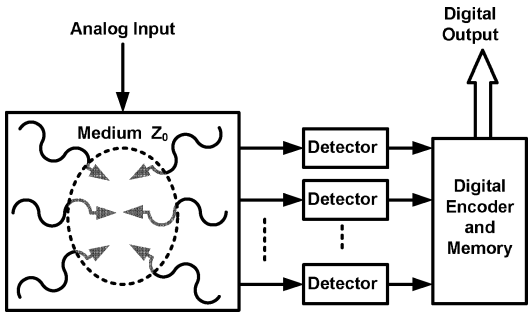

Fig. 1. 2-D lattice as an electrical interferometer.

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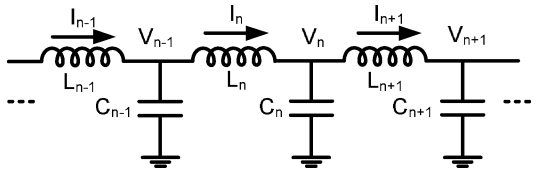

Fig. 2. Discrete 1-D transmission line.

detection. Since the amplitude of the pattern at these nodes matters, a power detector will be used to compare the power level with a certain threshold.

This paper is organized as follows. In Section II, we will review the behavior of waves in 1-D and 2-D LC lattices. The analysis of the proposed quantizer is presented in Section III. Finally, in Section IV, we propose the design methodology and present the simulation results.

II. Wave Propagation and Interference in Lattices

Let us consider a 1-D discrete transmission line made of inductors and capacitors, as shown in Fig. 2.

By applying Kirchoff's current law at node n, whose voltage with respect to ground is V_n, and applying Kirchoff's voltage law across the two inductors connected to this node, one can show that the voltages of adjacent nodes on this transmission line are related via

$$\frac{1}{L_n}(V_n - V_{n-1}) + C_n\frac{d^2V_n}{dt^2} + \frac{1}{L_{n+1}}(V_n - V_{n+1}) = 0. \quad (1)$$

This differential equation can be analytically solved if inductors and capacitors are identical [26]. For an inhomogeneous LC line where (1) is different for each section, a continuum model can be used to find the response. This model is based on the assumption that the electrical length of each section is considerably lower than the wavelength; thus, dispersion caused by discreetness is negligible. This approach has been used in [20] for analyzing an exponentially tapered transmission line with a constant L and C product. In this paper, we perform tapering by keeping the L/C ratio constant, thus minimizing fluctuation in the characteristic impedance Z_0. Keeping Z_0 constant ensures power matching along the line and consequently minimizes standing-wave formation, which can cause oscillation. Hence, keeping Z_0 constant reduces the settling time of the lattice in response to the input change.

A. Exponential Tapering With Constant L/C

In order to analyze a constant L/C tapering, we choose the inductance and capacitance of the nth section to be

$$\begin{aligned} C_n &= C_0\exp(\rho n) \\ L_n &= L_0\exp(\rho n) \end{aligned} \quad (2)$$

where ρ, C_0, and L_0 are constants. By substituting these values into (1) and assuming that the values of inductance and capacitance do not change abruptly between adjacent nodes ($\rho \ll 1$), we can use the continuum limit to obtain a single differential equation for the line. In this case, we can approximate (1) with respect to its spatial derivatives assuming that the node spacing is δ and the node location x is $n\delta$. By performing the Taylor series expansion of V_{n+1} and V_{n-1} around V_n and neglecting third-order and higher order terms, we can derive the continuum limit differential equation

$$\frac{d^2v}{dt^2} = -\frac{\exp(-2\mu x)}{l_0c_0}\frac{d^2v}{dx^2} \quad (3)$$

where $l_0 = L_0/\delta$ and $c_0 = C_0/\delta$ are unit length inductors and capacitors of the line, $\mu = \rho/\delta$ is the continuous tapering coefficient, and $v(x)$ is the continuum limit of V_n. Next, since Z_0 is constant, we assume a one-way traveling-wave solution

$$V(x,t) = A(x)\cos(\omega t - f(x)) \quad (4)$$

where we seek to find the function $f(x)$ that fits best to the phase-shift function. Inserting (4) into (3) results in

$$\begin{aligned} &-\omega^2 l_0c_0\cdot\exp(2\mu x)\cdot A(x)\cos(\omega t - f(x)) \\ &\quad = \cos(\omega t - f(x))\left[\frac{d^2A}{dx^2} - A(x)\left(\frac{df}{dx}\right)^2\right] \\ &\qquad + \sin(\omega t - f(x))\left[2\frac{dA}{dx}\cdot\frac{df}{dx} - A(x)\frac{d^2f}{dx^2}\right]. \end{aligned} \quad (5)$$

Based on sine and cosine coefficients, two independent equations can be derived from (5)

$$2\frac{dA}{dx}\cdot\frac{df}{dx} - A(x)\frac{d^2f}{dx^2} = 0 \quad (6)$$

$$-\omega^2 l_0c_0\cdot\exp(2\mu x)\cdot A(x) = \frac{d^2A}{dx^2} - A(x)\left(\frac{df}{dx}\right)^2. \quad (7)$$

Solving (6) leads to

$$\frac{df}{dx} = cA(x)^2 \quad (8)$$

where c is a constant. By replacing (8) into (7), we get a single differential equation in terms of $A(x)$

$$-\omega^2 l_0c_0\cdot\exp(2\mu x)\cdot A(x) = \frac{d^2A}{dx^2} - c^2A(x)^5. \quad (9)$$

Assuming smooth tapering in the line $\mu \ll 1$, we can assume second-order derivative of the amplitude to be small. Thus, by neglecting the first term in the right-hand side of (9), $A(x)$ can be solved as

$$A(x) = \sqrt[4]{\frac{\omega^2 l_0c_0}{c^2}}\cdot\exp(\mu x/2). \quad (10)$$

Consequently, by substituting (10) into (8), $f(x)$ can be derived as

$$f(x) = \frac{\sqrt{\omega^2 l_0c_0}}{\mu}\cdot\exp(\mu x). \quad (11)$$

Now we return to the discrete node analysis by replacing $x = \delta n$ in (4) and substituting $A(x)$ and $f(x)$ with $A(n)$ and $f(n)$

$$\begin{aligned} V_n(t) &= A(n)\cos(\omega t - f(n)) \\ A(n) &= \sqrt[4]{\frac{\omega^2 L_0C_0}{(\delta c)^2}}\cdot\exp(\rho n/2) \\ f(n) &= \frac{\sqrt{\omega^2 L_0C_0}}{\rho}\cdot\exp(\rho n). \end{aligned} \quad (12)$$

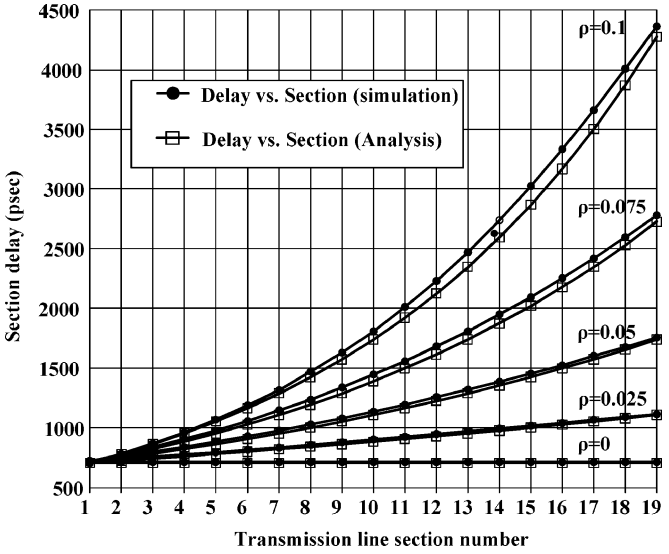

Fig. 3. Time delay versus section number in a 1-D tapered line for different tapering coefficients. Simulation is done with $L_0 = 50$ pH, $C_0 = 10$ fF, and $\omega = 2\pi \cdot 60$ GHz and it is compared with our analysis.

From (12) and by looking at the exponential terms, we can conclude that the variation in $A(n)$ is slow compared to $f(n)$; thus, for our further analysis, we neglect the amplitude variation across the line and only consider the phase variation. The delay per section can be found as

$$T_d(n)\cdot\omega = f(n) - f(n-1) \simeq \left.\frac{df(x)}{dx}\right|_{x=\delta n}\cdot\delta$$
$$T_d(n) = \sqrt{L_0C_0}\exp(\rho n). \tag{13}$$

Fig. 3 shows T_d for different values of ρ, where simulation closely follows our analysis.

We can furthermore elaborate on (12) by approximating $f(n)$ with a second-order polynomial for a small tapering coefficient. By only keeping the first three terms, we get

$$V_n(t) = A(n)\cos(\omega t - \phi_0 - k(n)\cdot n) \tag{14}$$

where ϕ_0 is a constant phase shift and

$$k(n) = \omega\sqrt{L_0C_0}\left(1 + \frac{\rho n}{2}\right) \tag{15}$$

is defined as the *effective wavenumber* at node n. From the above, we conclude that the exponential tapering will cause the wavenumber to increase (decrease) linearly along the line for positive (negative) values of ρ. This also means that we get a linearly decreasing (increasing) wavelength across the transmission line. Engineering the wavelength along the wave path is an effective way to change the topography of the interference pattern. We will exploit this property in designing interference patterns.

B. Interference Pattern in 1-D LC Ladders

Let us consider a 1-D discrete transmission line with N sections that is terminated with matched loads at both ends. We apply in-phase sources to the two ends and observe the interference pattern. The forward- and backward-propagating waves at node n can be written as

$$V_n^+(t) = \mathrm{Re}\{V_0\exp(j\omega t - j\gamma n)\}$$
$$V_n^-(t) = \mathrm{Re}\{V_0\exp(j\omega t - j\gamma[N-n])\}. \tag{16}$$

where γ is the complex propagation constant. By replacing γ with $\alpha + i\beta$, and applying superposition to the voltage node at the nth section of the line, the nodes' voltages are derived as

$$\begin{aligned} V_{\mathrm{tot}} &= \mathrm{Re}\{V_n^+ + V_n^-\} \\ &= V_0\cos(\omega t - \beta n)e^{-\alpha n} \\ &\quad + V_0\cos(\omega t - \beta(N-n))e^{-\alpha(N-n)} \\ &= V_0e^{-\alpha N/2}\Big[\cos(\omega t - \beta(N/2-n'))e^{-\alpha(N/2-n')} \\ &\qquad + \cos(\omega t - \beta(N/2+n'))e^{-\alpha(N/2+n')}\Big] \end{aligned} \tag{17}$$

where we define

$$n' = N/2 - n \tag{18}$$

in order to have a symmetric form around the center. Here, α is the loss of the line and β is the propagation constant for a lossless line. In (17), if the loss is small $(\alpha \ll 1)$ *or* if the nodes of interest are around the center of the transmission line $(n' \ll N/2)$, the two loss exponential terms in (17) are approximately equal. Thus, we can rewrite (17) as

$$V_{\mathrm{tot}} = 2V_0\exp(-\alpha N/2)\cos(\beta n')\cos(\omega t - \beta N/2). \tag{19}$$

The above equation shows that due to interference, the voltage amplitudes of the nodes are modulated across the line, by the periodic function, $\cos(\beta n')$.

The same analysis can be performed to find the interference pattern inside a tapered line. We consider a centrally symmetric tapering by choosing the values of inductors and capacitors as

$$C_n = C_0\exp(\rho|n'|)$$
$$L_n = L_0\exp(\rho|n'|). \tag{20}$$

As shown in Fig. 4, we can write the response of the transmission line to (16) as the sum of the transmitted and reflected waves in the two regions, where exponential tapering results of (14) are valid. In this case, the voltage of the line can be expressed as

$$V_{\mathrm{tot}} = \begin{cases} V_+^+\exp(-i\beta_{n'}n') + V_-^+\exp(i\beta_{n'}n'), & n < N/2 \\ V_+^-\exp(-i\beta_{n'}n') + V_-^-\exp(i\beta_{n'}n'), & n > N/2 \end{cases} \tag{21}$$

where

$$\beta_{n'} = \sqrt{L_0C_0}\omega(1 + \rho N/4 - \rho|n'|/2) \tag{22}$$

is the varying propagation constant, which is the same as $k(n)$ in (14). Since the characteristic impedance is kept constant across the line, no reflection happens at the center boundary, which means $V_+^+(n = N/2) = V_-^-(n = N/2)$ and $V_-^+(n = N/2) =$

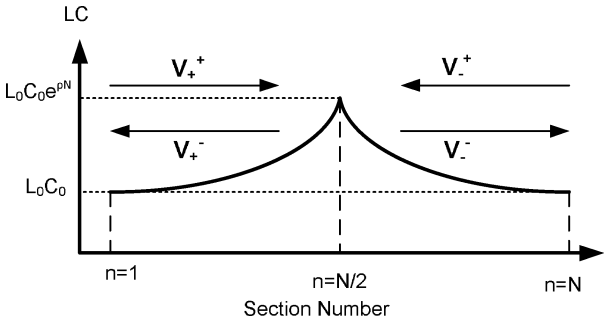

Fig. 4. Incident and reflected waves across the two sections of the tapered 1-D transmission line.

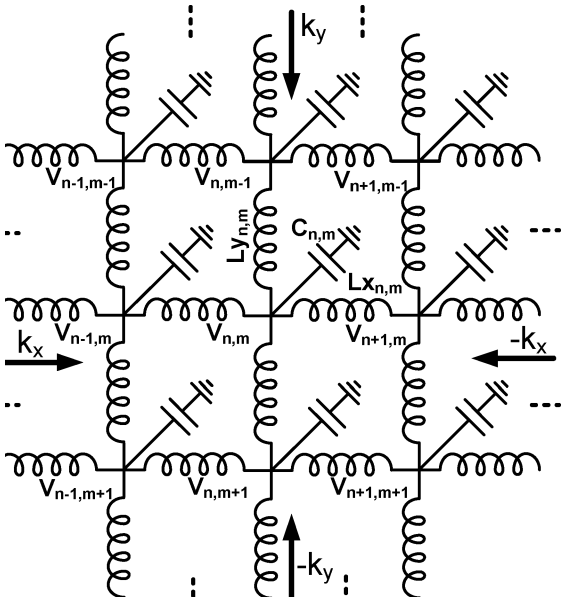

Fig. 5. Discrete 2-D transmission lattice.

$V_+^-(n = N/2)$. By applying this condition and the boundary conditions at two ends of the line, the solution becomes

$$V_{\text{tot}} = 2V_0 \cos(\beta_{n'} n') \cos(\omega t - \beta_{n'} N/2). \tag{23}$$

This solution is quite similar to (19), when we replace β with $\beta_{n'}$. We did not consider the effect of loss in the tapered line, but by comparing (23) to the uniform line result of (19), we can observe that the loss should similarly result in an amplitude peak lower than $2V_0$.

C. Generalization to 2-D

A 2-D lattice composed of inductors and capacitors is shown in Fig. 5. This lattice gives more degrees of freedom in designing circuits as compared with a 1-D line. Although feeding the input to a 2-D lattice is more complicated than a 1-D transmission line and requires a power division network, for a given number of inductors, the propagation length from the edge of the 2-D lattice to its center is much less than a 1-D transmission line, which makes 2-D structures more desirable in the presence of loss.

In this lattice, we assume that all four sides are terminated to matched loads. In addition, we assume an $N \times M$ rectangular lattice and apply in-phase signal sources to all four boundaries. Assuming no reflection on the sides, we can write the effect of all four waves at each node of the lattice as

$$\begin{aligned} V_{n,m}(t) = \text{Re}\{&V_0 \exp(i\omega t - ik_x n) \\ &+ V_0 \exp(i\omega t - ik_x (N-n)) \\ &+ V_0 \exp(i\omega t - k_y m) \\ &+ V_0 \exp(i\omega t - k_y (M-m))\} \end{aligned} \tag{24}$$

where k_x and k_y are the propagation constants in the two perpendicular directions. Since the four plane waves of the right side of (24) only propagate in the x- or y-direction, we can treat them as the solutions of orthogonal 1-D transmission lines. Using a change of variable,

$$\begin{aligned} n' &= N/2 - n \\ m' &= M/2 - m \end{aligned} \tag{25}$$

(24) is simplified to

$$\begin{aligned} V_{n,m}(t) = &2V_0 \cos(-k_x N/2) \cos(k_x n') \\ &+ 2V_0 \cos(-k_y N/2) \cos(k_y m'). \end{aligned} \tag{26}$$

If the lattice is central symmetric (i.e., $k_x = k_y = k$ and $N = M$), (26) becomes

$$\begin{aligned} V_{n,m}(t) = &4V_0 \cos\left(k\frac{n'+m'}{2}\right) \\ &\times \cos\left(k\frac{n'-m'}{2}\right) \cos(\omega t - kN/2). \end{aligned} \tag{27}$$

The solution has a constant envelope $(4V_0)$, modulated by two diagonal periodic functions. This 2-D modulation provides a pattern that is well suited for the purpose of our quantizer.

III. Interferometric Quantization

Based on our analysis in Section II, we propose a method for efficiently changing the interference pattern of an LC lattice using MOS varactors. The change in the capacitors will change the propagation constant and wavelength, which will in turn change the voltage across lattice nodes. This change in the voltage across the lattice will be detected for the purpose of signal quantization.

A. MOS Varactor

A MOS varactor is a device operating in depletion or accumulation mode, where changing the gate voltage changes the effective capacitance [29]. The C–V curve of an accumulation mode MOS varactor is shown in Fig. 6. The small-signal capacitance is defined as

$$C = \frac{dQ}{dV}. \tag{28}$$

For small variations, the C–V characteristic of Fig. 6 can be approximated as

$$C(V) = \frac{C_0}{(1 - bV)} \tag{29}$$

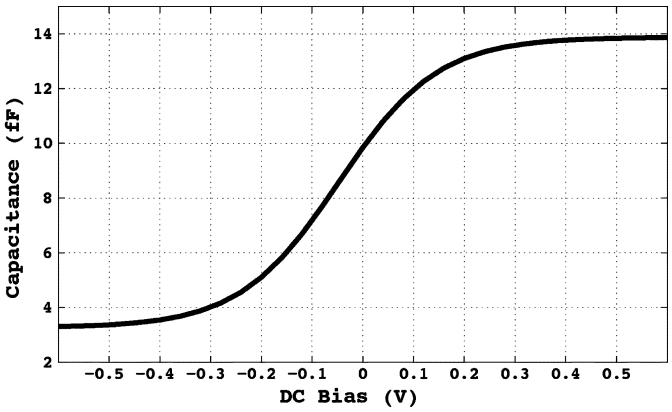

Fig. 6. Characteristic of an accumulation mode MOS varactor.

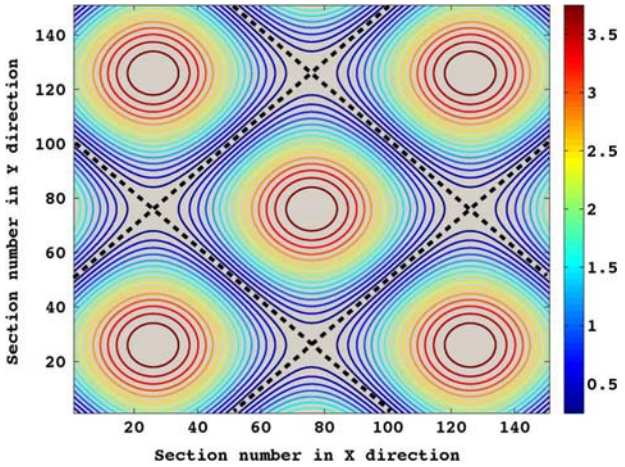

Fig. 7. 2-D lattice interference pattern and its central lobe. The contours represent nodes of the lattice with equal voltage amplitudes and the dashed lines represent nodes with zero amplitude. The voltage levels are normalized with respect to the input voltage level.

where V is the bias voltage across the varactor and C_0 and b are constants.

Even though (29) describes a nonlinear system, for small input amplitudes around a bias voltage of V_c, we can neglect the effect of nonlinearity and approximate the current across the capacitor by

$$I \approx \frac{C_0}{(1-bV_c)}\frac{dV}{dt} = C(V_c)\frac{dV}{dt}. \tag{30}$$

Thus, if capacitances in Fig. 2 are replaced by varactors, we can simply rewrite (1) by replacing all capacitors with the varactor small-signal capacitance $C(V_c)$. Based on this linear model, we use varactors to change wave propagation and its interference pattern in an LC lattice.

B. 2-D Lattice Quantization

In the $N \times N$ 2-D lattice described in Section II, if we replace the capacitors with varactors, the voltage swing at the nth row and mth column would be

$$V_{n,m} = 4V_0 \cos(\omega t - k(V_c)N/2) \cdot \cos\left[k(V_c)\frac{n'+m'}{2}\right]\cos\left[k(V_c)\frac{n'-m'}{2}\right] \tag{31}$$

where

$$k(V_c) = \sqrt{L_0\frac{C_0}{(1-bV_c)}}\omega. \tag{32}$$

We propose the following quantization method.

1) Apply a sample of the analog signal to the bottom plate of the varactors, resulting in a change of their capacitance by changing the bias point $V_c = V_{\text{in}}$.
2) Apply small-signal in-phase sinusoidal inputs to all sides of the lattice.
3) Four plane waves generated by the input sources propagate inside the lattice and form the interference pattern. This pattern depends on the value of the varactors, and hence, is a function of the analog signal.
4) Using a power detector, we detect the output power at *certain* nodes of the lattice.
5) The detected output is compared with a threshold level, V_T. The nodes above V_T are defined as logic 1, and the nodes below it are defined as logic 0.
6) The total number of logic 1 outputs, S_{tot}, is the digital output code.

In order to show how S_{tot} is related to the analog signal, we need to know which outputs are suitable for this kind of quantization. There is no unique way to select the output as long as a monotonic relation between the analog input and the quantized output holds. We will show that by using the lattice nodes at the first lobe of the interference pattern (in the center of the lattice), we obtain the desired relationship. We can find other selection sets that can result in the same relation, but in terms of implementation it is desirable to have processing nodes close to each other to minimize routing issues and to share similar circuit blocks. Also, from loss analysis done in Section II, we concluded that the effect of loss on the amplitude modulation will be negligible at the central nodes.

A typical interference pattern for a uniform 2-D lattice is shown in Fig. 7. The first interference lobe is surrounded by the dashed lines in the center of the lattice. We are interested in finding the number of nodes that satisfy $V_{n,m} > V_T$ inside this region. From (31), the first lobe can be mathematically described as

$$-\frac{\pi}{2} \le k(V_{\text{in}})\frac{n'+m'}{2} \le \frac{\pi}{2}$$
$$-\frac{\pi}{2} \le k(V_{\text{in}})\frac{n'-m'}{2} \le \frac{\pi}{2}. \tag{33}$$

For the nodes close enough to the center, we can perform a Taylor series expansion on the voltage waveform of (31) with respect to $n'+m'$ and $n'-m'$ and neglect third-order and higher order terms to obtain

$$4V_0(1-k(V_{\text{in}})^2 \cdot \frac{n'^2+m'^2}{4} + O(n^4)) > V_T. \tag{34}$$

Neglecting higher order terms and substituting (32) into (34), we have

$$n'^2 + m'^2 < [1-bV_{\text{in}}]\frac{\omega_T^2}{\omega^2} \cdot \left(1-\frac{V_T}{4V_0}\right) \tag{35}$$

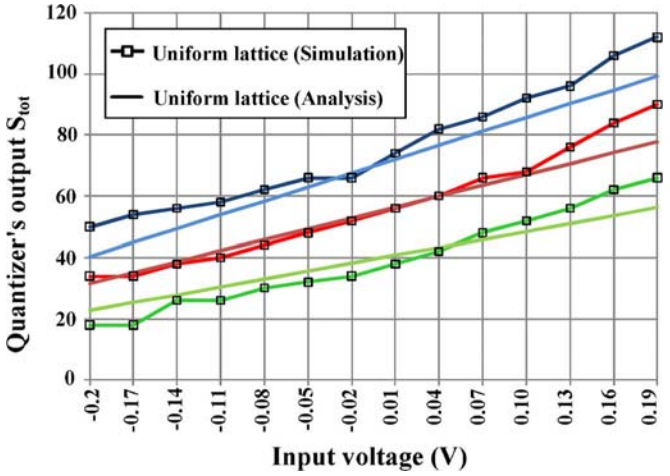

Fig. 8. Analysis versus circuit simulation of the quantizer input–output relation for a uniform lattice with $L_0 = 56$ pH and C_0, as in Fig. 6. The comparison is performed for $V_T = 70$ mV (blue in online version), $V_T = 80$ mV (red in online version), and $V_T = 90$ mV (green in online version). In order to take into account the effect of loss in the analysis, a smaller input swing is a applied to (37).

where

$$\omega_T = \frac{2}{\sqrt{L_0 C_0}} \tag{36}$$

is the lattice cutoff frequency in the orthogonal direction. Note that in 2-D lattices ω_T depends on the wavefront direction [27]. The nodes that satisfy (34) are within a circle with a radius R equal to the square root of the right-hand side of (35). The number of nodes inside this circle is equal to its area

$$S_{\rm tot}(V_{\rm in}) = \lfloor \pi R^2 \rfloor = \left\lfloor \pi[1 - bV_{\rm in}]\frac{\omega_T^2}{\omega^2} \cdot \left(1 - \frac{V_T}{4V_0}\right) \right\rfloor. \tag{37}$$

Thus, the quantized output code is, approximately, linearly proportional to the input analog voltage. Note that the proportionality factor will be

$$\frac{\Delta S_{\rm tot}}{\Delta V_{\rm in}} \approx \frac{d(\pi R^2)}{dV_{\rm in}} = -b\pi\frac{\omega_T^2}{\omega^2} \cdot \left(1 - \frac{V_T}{4V_0}\right). \tag{38}$$

From the above, we can conclude that the quantizer will have higher resolution when capacitor variation (b) is higher, the operating frequency is much less than the cutoff, and the threshold voltage (V_T) is lower. As shown in Fig. 8, simulation results follow the predicted behavior in (37) with minor deviations, which is mostly due to the linear and continuum approximations we made through the analysis.

It is worth mentioning that the circular region is accurate when the threshold voltage is close to the peak voltage $4V_0$. As the threshold increases, the circular region gradually transforms to a rectangular region. This transformation can be clearly seen in the constant envelope contours of Fig. 7. For $V_T = 0$, we have

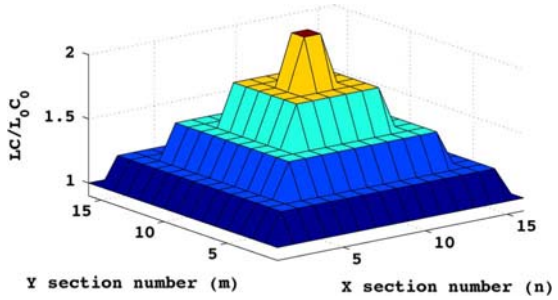

Fig. 9. 2-D lattice with central symmetric LC tapering.

the whole square-shaped central lobe, with its diagonal equal to the wavelength λ, and we can write

$$S_{\rm tot}(V_{\rm in}) = \left\lfloor \frac{\lambda^2}{2} \right\rfloor = \left\lfloor \pi^2[1 - bV_{\rm in}]\frac{\omega_T^2}{2\omega^2} \right\rfloor \tag{39}$$

$$\frac{\Delta S_{\rm tot}}{\Delta V_{\rm in}} \approx -b\frac{\pi^2}{2}\frac{\omega_T^2}{\omega^2}. \tag{40}$$

This result is slightly different than (38) in the proportionality factor, but the input–output relation is similar.

C. Effect of Tapering

The above analysis is based on a uniform lattice, but this is not necessarily the best implementation. Since we are only interested in the central lobe of the interference pattern, a uniform tapering is not optimum. In Section II, we showed that a constant L/C ratio tapering in 1-D gradually decreases the wavelength, which means that the interference pattern has a shorter wavelength at the center. In other words, the central lobe is *focused* with respect to other lobes.

In a 2-D lattice, by applying this tapering in both dimensions, for a positive ρ, the central lobe becomes smaller and more focused, while for a negative ρ, the central lobe becomes larger and more dispersed. In Fig. 9, such a central symmetric tapering with a positive ρ is shown. We can use tapering to get better resolution on the nodes of interest.

IV. Quantizer Design and Simulation

In order to get the best performance out of the proposed quantizer, we need to optimally design different aspects of the structures. From (38), the quantization factor is a strong function of the ratio of the lattice cutoff frequency to the carrier frequency, and a higher ratio provides a better resolution.

On the other hand, the lattice response time plays a major role in the overall quantization speed. Since we maintain matching conditions in the entire lattice, reflection over the boundaries is minimal. Hence, the time it takes for the lattice to respond to a change in the analog input will be the time it takes for the wave to travel through the lattice sections. For frequencies reasonably below the cutoff, we can write this time as

$$T_D = \sum_{i=1}^{N} \sqrt{L_i C_i} \tag{41}$$

where L_i and C_i are the inductance and capacitance of the ith section, respectively. One can achieve the fastest response time by setting L_i's equal to L_0 and C_i's equal to C_0

$$T_{\min} = \sum_{i=1}^{N} \sqrt{L_0 C_0} = \frac{2N}{\omega_T} \tag{42}$$

where we have substituted for ω_T from (36). Note that, if the nodes of interest are close to the center of the lattice, only half of the lattice sections count to the overall delay, which will significantly reduce the response time.

Equations (38) and (42) suggest that a higher ω_T will result in higher resolution and higher speed, respectively. Thus, the reasonable way to design the lattice is to choose ω_T to be the highest possible value implementable in a certain technology. In a properly designed structure, because of the high cutoff frequency of the lattice, we expect the rest of the circuit, including the power detector and the memories, to be the overall limiting factor. For this study, we use TSMC's 65-nm standard CMOS technology, and we use Cadence for the simulations [31].

A. 2-D Lattice

The 2-D lattice shown in Fig. 5 gives us a vast degree of freedom in choosing the inductors and capacitors as long as the L/C ratio remains constant everywhere. We start by choosing C_0 and L_0 for a maximum ω_T. The lowest possible varactor in the process with minimum dimensions has an average C_0 of around 9 fF. Below this value, the parasitic capacitance becomes significant. The characteristic of this varactor is shown in Fig. 6. Furthermore, we select $L_0 = 56$ pH since this is the smallest lumped inductor that is modeled in the process. Customary inductors smaller than this value can also be designed by performing extensive electromagnetic modeling and simulation. With these values, the characteristic impedance of the line will be $Z_0 = \sqrt{L_0/C_0} = 78\,\Omega$, which is a practical value for implementation. Also, from (36), $f_T = \omega_T/(2\pi) = 425$ GHz, which is much higher than carrier frequencies that CMOS devices can handle. Thus, the signal wavelength is much shorter than the lattice spacing and our analysis based on a continuum model is valid.

In order to estimate the effect of loss in the lattice, the quality factors of the inductor (Q_L) and capacitor (Q_C) are plotted in Fig. 10 In a continuum approximation, for the lattice quality factor, we have $Q = \beta/(2\alpha)$, where

$$\alpha = \frac{\omega\sqrt{L_0 C_0}}{2}\left(\frac{1}{Q_L} + \frac{1}{Q_C}\right) \tag{43}$$

and

$$\beta = \frac{1}{\sqrt{L_0 C_0}} \tag{44}$$

are the real and imaginary parts, respectively, of the propagation constant γ [28]. The loss of the varactor is clearly dominant for high frequencies and will dominate the overall lattice quality factor. We concluded from our analysis in Section III that in order to have an effective interference pattern formation, loss should be small, and simulation results suggest that a quality factor higher than 5 is required for an effective interference pattern formation. As a result, from Fig. 10, we choose our carrier frequency to be 60 GHz.

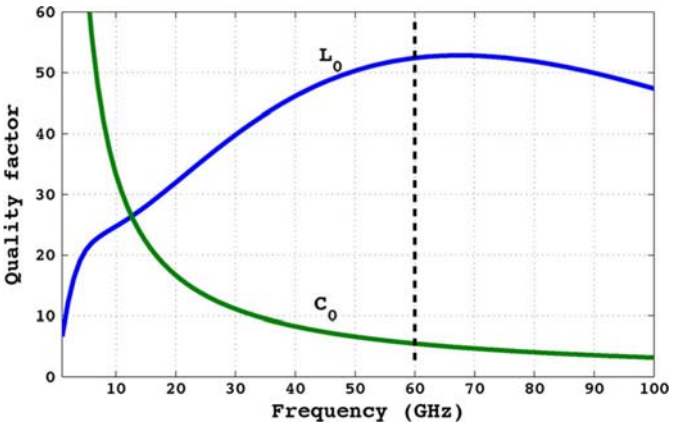

Fig. 10. Inductor and capacitor quality factor versus frequency. The design point is shown by the dashed line.

The next step is to decide on lattice dimensions and any possible tapering. From our analysis in Section III, and as a rule of thumb, we desire to have the entire central lobe of the interference pattern inside the lattice. Thus, from Fig. 7 and (39), the dimensions should be around λ, or

$$N = \pi\frac{\omega_T}{\omega}. \tag{45}$$

For $f_T = 425$ GHz and $f = 60$ GHz, we get $N = 23$. This is a relatively large number considering the amount of loss in the lattice. Furthermore, since power splitting is more efficient for powers-of-2 numbers of inputs, we choose $N = 16$ as the closest one and will use tapering in order to focus the pattern in this smaller dimension.

Although from Fig. 10, going to lower frequencies enhances the lattice quality factor, but because the detector needs few periods of the carrier frequency to detect the voltage level, the carrier frequency needs to be higher than the sampling frequency. This is to say that the maximum value of the carrier frequency is set by the quality factor of the varactors and its minimum is determined by the speed of the detectors. In order to estimate the maximum achievable sampling rate, we should take into account both the lattice delay T_D and the detection time. By dedicating two periods of the carrier for the detector, we can estimate the maximum sampling rate as

$$F_S = \frac{1}{T_D + 2/f}. \tag{46}$$

The fastest sampling rate can be achieved in a uniform lattice, where for $T_D = T_{\min}$, we get $F_{S\max} = 22$ GS/s. Due to tapering in our final design, T_D becomes slightly higher than $T_{\min}$. However, the detector response time remains as the limiting factor in (46); thus, we choose a 50-ps response time corresponding to $F_S = 20$ GS/s for this design.

From our discussion in Section II, a tapered line with $\rho > 0$ decreases the wavelength, and we expect a smaller lobe compared with a uniform profile. Our simulation results show in Fig. 11 that $\rho = 0.09$ is sufficient to fit the first lobe into the

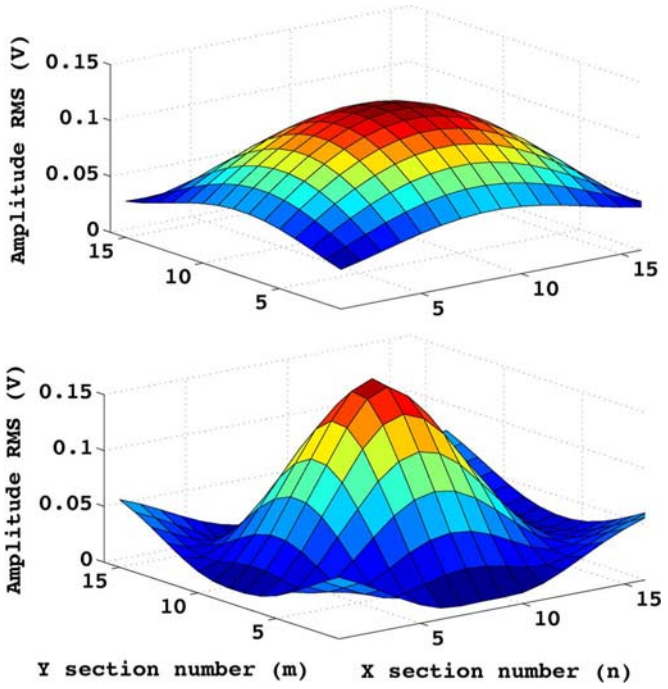

Fig. 11. Uniform versus tapered lattice output. (*top*) Uniform lattice with $L = L_0$ and $C = C_0$. (*bottom*) Constant L/C tapered lattice with tapering factor of $\rho = 0.09$. The tapered lattice focuses the first interference lobe to fit inside the 16×16 lattice. Simulation is done with source amplitudes of 50 mV.

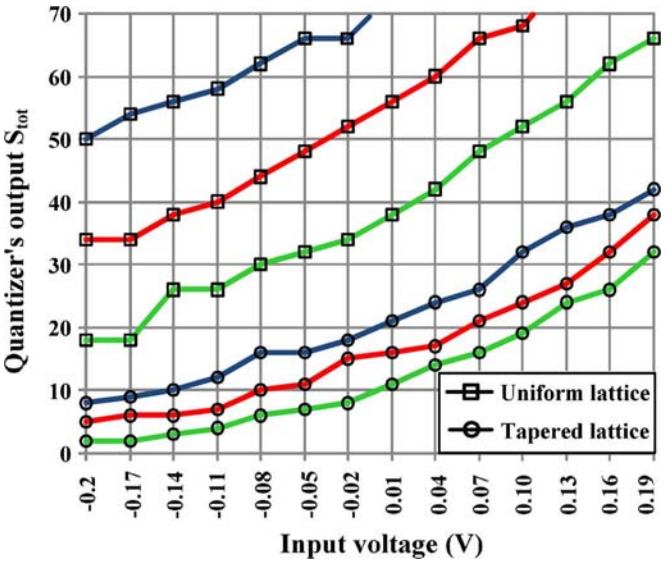

Fig. 12. Quantizer's output characteristic with and without tapering. All inputs are ideal matched sources with input amplitude of 50 mV. The simulation is done for $V_T = 70$ mV (blue in online version), $V_T = 80$ mV (red in online version), and $V_T = 90$ mV (green in online version). We observe the effect of tapering, which is focusing the variation in a smaller number of nodes while maintaining the desired input–output trend.

16×16 lattice. Also from Fig. 11, the tapering gives a larger peak amplitude, which is desirable in the detection process.

Fig. 12 shows the quantized output versus the analog input for different V_T's. By performing simulations with different threshold levels, V_T, we can choose the best value for our design. In this design, we choose $V_T = 90$ mV to get a sufficiently large dynamic range.

B. Specifying the Input–Output Characteristic

The derived characteristic of Fig. 12 is assuming that all lattice nodes outputs in the first lobe are counted. This is neither practical, nor useful considering the resulting input–output curve, which is not desirable for many ADC applications. For a more practical input–output characteristic, we will choose a subset of these nodes. An input–output curve, $S_{\rm sub}(V_{\rm in})$, can be extracted from the original curve provided that

$$0 \leq \frac{\Delta S_{\rm sub}}{\Delta V_{\rm in}} \leq \frac{\Delta S_{\rm tot}}{\Delta V_{\rm in}}. \tag{47}$$

For any curve satisfying (47) across the whole input range, the total number of node transitions from logic 0 to logic 1 at desired input levels $\Delta S_{\rm tot}/\Delta V_{\rm in}$ are equal or more than the required number $\Delta S_{\rm sub}/\Delta V_{\rm in}$. Thus, one should select the subset of desired transition points and the nodes corresponding to them. In transition points that more than one node is there to choose from, we tend to choose the nodes in a uniform pattern across the lattice. This will minimize the loading effect of the detectors on the lattice characteristic impedance. Fig. 13(a) shows a 16-level (4 bit) linear characteristic, satisfying (47), achieved by choosing only 16 nodes of the lattice.

Even though a linear quantizer is usually used for communication applications, other characteristics may also be desired. Some signals tend to occur more frequently at low amplitudes, which makes a saturating characteristic more optimal for their quantization [30]. In order to show this possibility, a saturated quantizer is designed, as shown in Fig. 13(b). Also, by dynamically changing the selection set, we have the ability to dynamically change the quantizer's characteristic, which can be potentially very useful. As an example, in RF receivers where the received signal power changes from time to time, we can use a variable quantizer in addition to the variable-gain amplifiers to dynamically tune the total gain of the signal path.

C. Detector and Memory

Fig. 14 shows the detector circuit, which is composed of two parallel self-mixers. The input node with amplitude $V_{\rm in}$ is connected to M_1, M_6, and M_7. Since the input node is single-ended, the other three nodes are connected to bias voltages. The reference signal with an amplitude V_T is applied to the other mixer through M_3, M_{10}, and M_{11}. The output voltage is proportional to $V_{\rm in} - V_T$ with a proportionality factor depending on devices' transconductances. The width and length of M_{1-12} are 4 μm and 60 nm, respectively. We have designed the detector by simultaneously minimizing its loading on the lattice and its response time.

The sign of the differential output is the actual logic level of the detector. From this point, since the differential output is still small, we will amplify the signal to the desired level. In order to maximize the sampling speed, we propose a pipeline amplification technique. In this method, the output of the detector is applied to a cascade of sampled mode gain stages. Each gain stage samples the output of the previous stage, amplifies it to the maximum possible level during the time window, and provides the higher voltage level to the next stage. In Fig. 15, one such stage is shown in which the output of the Nth stage is sampled on a capacitor and at the next phase it is applied to the $(N+1)$th

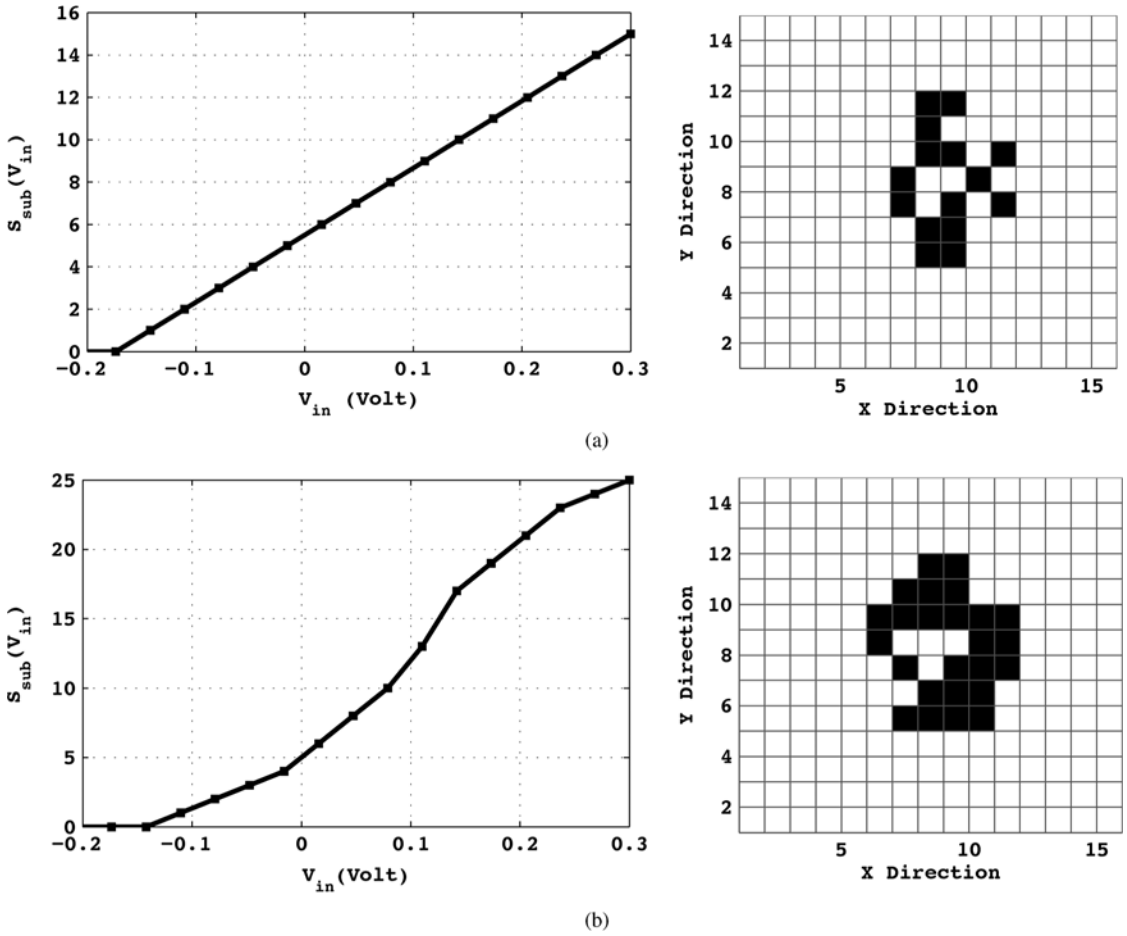

Fig. 13. Quantizer output versus input voltage for two different selection sets showing two examples of various achievable input–output characteristics. (*top left*) 16-level or 4-bit linear quantizer. (*top right*) Its selection set for output nodes. (*bottom left*) Logarithmic (saturating) quantizer. (*bottom right*) Its selection set for output nodes.

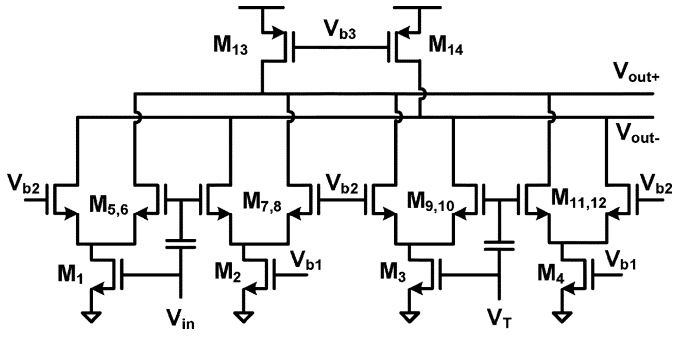

Fig. 14. Voltage detector circuit with input and reference inputs and the differential output.

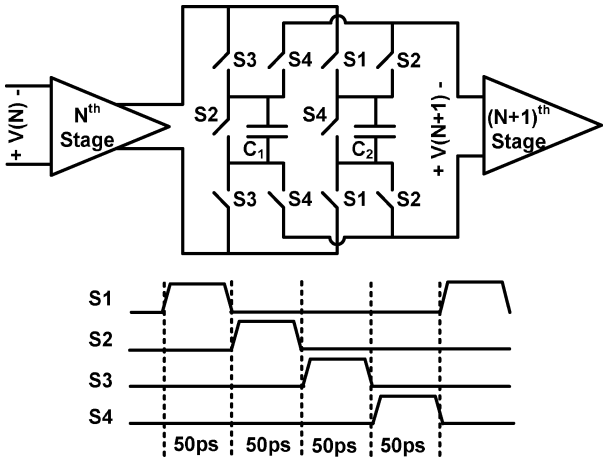

Fig. 15. Nth stage of the cascaded amplification circuit with the switches and the four clock phases.

stage. Capacitors C_1 and C_2 are both 5 fF and they sample the signal in turns, meaning that while one is sampling, the other is being reset. The switched capacitors are controlled by NMOS switches with phases S_1 to S_4.

This technique is, in fact, a high-speed analog shift register, in which the logic bit is shifted and amplified across the stages and the gain stages can also be considered as part of the memory. The gain stages are designed for maximum gain in the provided 50-ps settling time. A two-stage differential pair shows optimum functionality for each gain stage. The transient response of the detector and the first two gain stages are shown in Fig. 16. The results show that the detector output response is fast enough to be sampled in the 50-ps time window. Fig. 17 shows the time-domain simulation of the lattice connected to

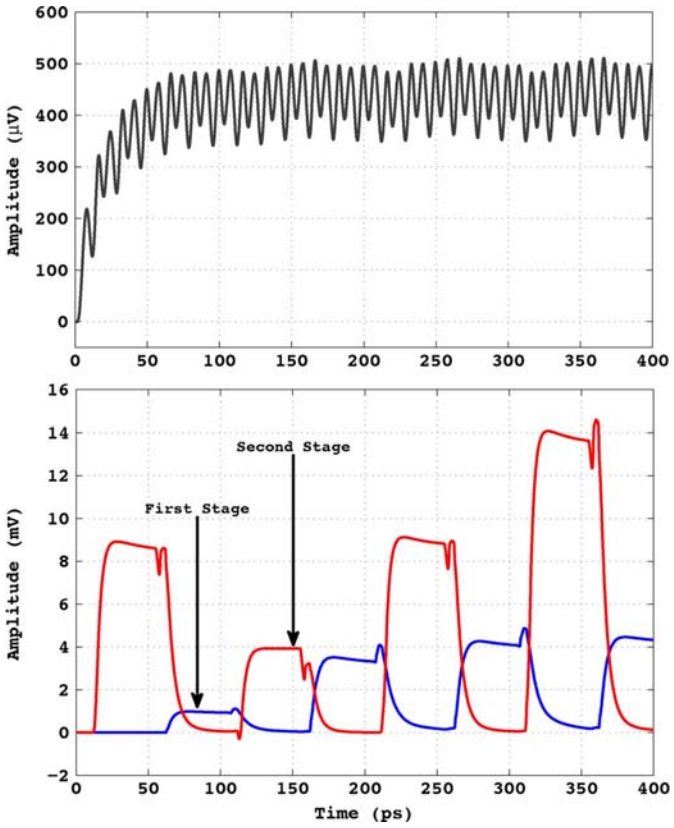

Fig. 16. (*top*) Detector's transient response for $V_{\rm in} = 55$ mV and $V_T = 50$ mV. (*bottom*) First gain stage (blue in online version) and second gain stage (red in online version) sampled voltages for the above detector output. The first gain-stage samples the detectors output and amplifies it in a 50-ps time window. For the next 50 ps, the second stage amplifies the previous output, while the fist stage is being reset. The sign of the detector output is the logic state, which, in this case, is positive ($V_{\rm in} > V_T$).

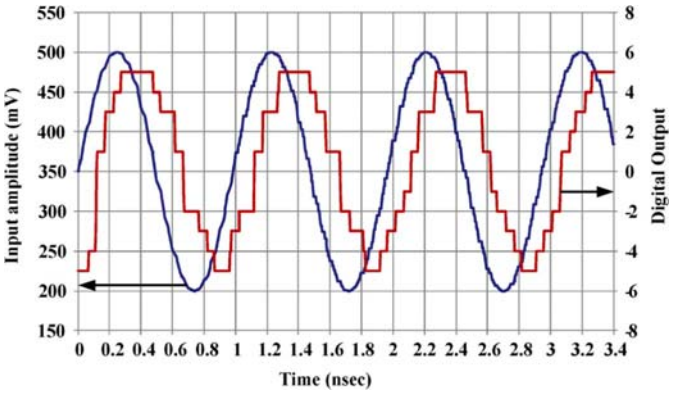

Fig. 17. Time-domain simulation. Input sinusoid at 1.7 GHz (blue in online version) and the digital output (red in online version). All other parameters are the same as the constant input simulations we performed before.

the detector circuit. The corresponding spectrum of the digital output is plotted in Fig. 18.

D. Design Summary and Comparison

We showed that with a 16×16 tapered lattice we can achieve at least 4 bits of linear quantization. The detector circuit's response time combined with the lattice delay from (46) achieves

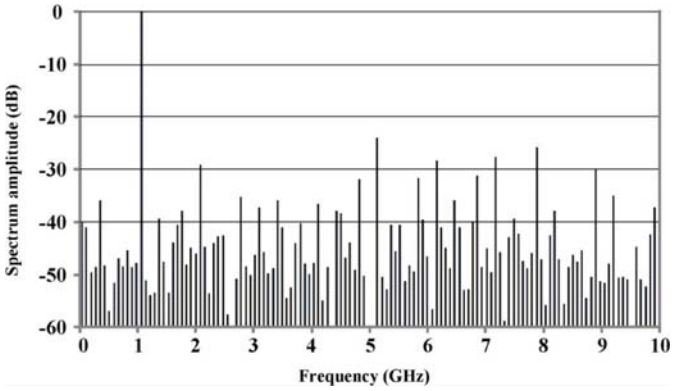

Fig. 18. Digital output fourier transform for 256 samples of the output.

a sampling rate of 20 GS/s. The dc current of the detector is 5 mA from a 1.2-V supply, and with double sampling performed to achieve the desired sampling rate, each detection node consumes 10 mA of current. The gain stage amplifiers consume 3 mA each. The number of gain stages used depends on the logic output level required for the memory. For our design, we require detection of $V_{\rm in} - V_T > 1$ mV, and from simulation, for $V_{\rm in} - V_T = 1$ mV, the detector output is around 50 μV after 50 ps. Thus, to achieve an output level as large as 0.2 V, the number of stages will be

$$N_s = 2 \times \left(\log_{3.5}^{0.2} - \log_{3.5}^{50\mu} \approx 13 \right) \tag{48}$$

where, similar to the detection part, the factor of 2 comes from double sampling. The power required to drive the 16×16 lattice at all four sides for the 50-mV input amplitude is

$$P_{\rm lattice} = 4 \times 16 \times \frac{V^2}{Z_0} = 2\,\text{mW}. \tag{49}$$

The total detection power is the sum of the detector and the lattice power

$$P_{\rm detection} = P_{\rm lattice} + 16 \times 10\,\text{mA} \times 1.2\,\text{V}. \tag{50}$$

Table I compares the proposed quantizer with other reported designs. The comparison is performed both with and without taking into account the analog memory. The reason is that the memory is not the essential part for the detection, and as soon as the output is quantized, the data can be stored in many ways. For example, time interleaving can be used to design a memory with a considerably lower sampling rate and power consumption.

It is noteworthy that we do not have measurement results of this structure and the comparison might not be fair. As a result, we do not draw any conclusions beyond the fact that this structure shows great potential as a high-speed power-efficient quantizer.

E. Effect of Noise and Phase Mismatch

The main effects that can degrade the performance of the interferometric quantizer are thermal noise and phase mismatch between input sources. Thermal noise is caused by the source impedance and also the detector circuit, while phase mismatch

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART ADCs

Ref.	Architecture	Quantizer Power	Total Power	F_s	Resolution	Technology
[3]	Time interleaving	N/A	1.2W	24G	6 bits	90*nm* CMOS
[4]	Time interleaving	N/A	9W	20G	8 bits	0.18μm CMOS
[6]	Flash	N/A	4.5W	35G	4 bits	SiGe BiCMOS
[7]	Flash	N/A	4.8W	20G	5 bits	SiGe BiCMOS
[8]	Flash	N/A	3.6W	10G	5 bits	SiGe BiCMOS
This Work	Interferometer	0.194W	0.943W	20G	4 bits	65*nm* CMOS

between the inputs happen randomly mostly due to process variation across the substrate. To capture both of these effects, we model the ith input source as

$$V_i = (V_0 + v_i)\cos(\omega t + \theta_i) \tag{51}$$

where v_i is the additive white Gaussian noise and θ_i is a random phase. For θ_i, we assume a Gaussian distribution with zero mean and variance of σ_θ. From our analysis in Section II-C, the voltage of any node inside the 2-D lattice is a superposition of four input sources that are in the same column and row as that node. This is assuming that the phase mismatch between sources on one edge of the lattice is not large, and hence, the direction of the wave is not significantly changed. By applying the nonideal sources of (51) to (24), we can write the voltage of each node as

$$V_{n,m} = \sum_i \left[(V_i + v_i)\cos(\omega t - \Delta\phi_i + \theta_i)\right] \tag{52}$$

where we have given indices to the independent noise and mismatch sources and $\Delta\phi_i$ represents the phase shift due to the wave propagating along the lattice. Assuming that $v_i \ll V_0$ and $\sigma_\phi \ll 1$, we can simplify the superposition of the four nodes from (52) to

$$\begin{aligned} V_{n,m} = {} & 4V_0 \cos\left(k\frac{n'+m'}{2}\right)\cos \\ & \times \left(k\frac{n'-m'}{2}\right)\cos(\omega t - k(V_c)N/2) \\ & + \sum_i \cos(\omega t - \Delta\phi_i) \\ & \cdot v_i - \sum_i V_0 \sin(\omega t - \Delta\phi_i)\cdot\theta_i. \end{aligned} \tag{53}$$

The first term in (53) is the desired amplitude coming from (27), while the next two term are the effect of noise and phase mismatch, respectively. We now substitute (53) into (34) and follow the same approximation to get the quantizer output $S_{\rm tot}$, shown in (54), at the bottom of this page. In order to find the signal to noise plus distortion ratio (SNDR), we calculate the output power by assuming independent noise and mismatch sources. We replace noise terms with noise power of $\overline{v_n^2}$ and mismatch terms with $\overline{\sigma_\phi^2}$ to get

$$\begin{aligned} \overline{S_{\rm tot}^2(V_{\rm in})} = {} & \pi^2\frac{\omega_T^4}{\omega^4} \\ & \times \left(1 + b^2\overline{V_{\rm in}^2}\left(1 - \frac{V_T}{4V_0}\right)^2 + \frac{2\overline{v_n^2} + 2V_0^2\overline{\sigma_\phi^2}}{16V_0^2}\right). \end{aligned} \tag{55}$$

The SNDR can be calculated from (55) by taking into account the signal and noise powers

$$\text{SNDR} = 8b^2(V_0 - V_T/4)^2 \cdot \frac{\overline{V_{\rm in}^2}}{\overline{v_n^2} + V_0^2\overline{\sigma_\phi^2}}. \tag{56}$$

Form (56), one can find the requirement on noise and phase mismatch for a particular SNDR. Fig. 19 shows the relation between these two noise sources for achieving a desired SNDR based on our analysis.

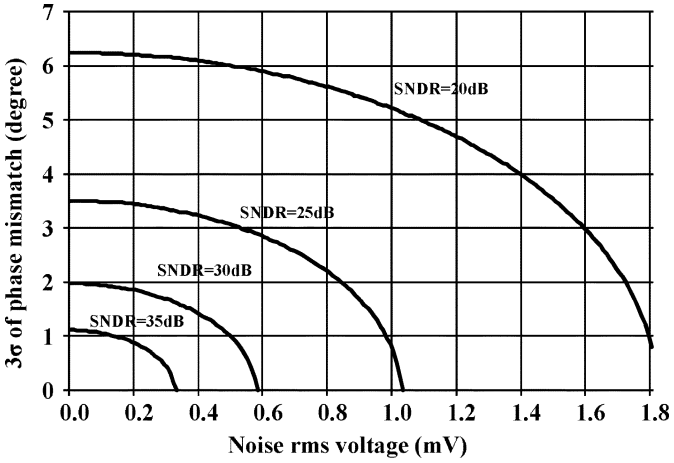

Fig. 19. Noise and mismatch limits for different values of SNDR. The lattice parameters are as specified in Section IV-D. The input $V_{\rm in}$ is assumed to be a sinusoid with an amplitude of 150 mV.

V. CONCLUSION

2-D electrical lattices have been used in signal generation and processing. By engineering the lattice and changing its properties with an analog input, we can form various interference pat-

$$S_{\rm tot}(V_{\rm in}) = \left\lfloor \pi(1 - bV_{\rm in})\frac{\omega_T^2}{\omega^2}\cdot\left(1 - \frac{V_T - \sum_i \cos(\omega t - \Delta\phi_i)\cdot v_i + \sum_i V_0 \sin(\omega t - \Delta\phi_i)\cdot\theta_i}{4V_0}\right)\right\rfloor \tag{54}$$

terns that can be exploited for high-speed signal quantization. We described the theory of interference in 2-D lattices, pattern formation, and the effect of lattice tapering. Next, we designed and simulated a 4-bit 20-GS/s quantizer in a 65-nm CMOS technology. This is the first proposed quantizer in CMOS at this sampling rate without time interleaving. It also has a remarkably low power consumption as compared to conventional structures and shows potential in low power detection of very high-speed signals.

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